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Research and Development on Advanced Silicon Carbide Thin Film Growth Techniques and Fabrication of High Power and Microwave Frequency Silicon Carbide-Based Device Structures

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13. ABSTRACT (Maximum 200 words)

Thin films of pure and Al-doped β-SiC have been grown on 4° off-axis Si(100) and c-axis oriented α(6H)-SiC in the temperature range of 1025–1250°C using gas-source molecular-beam epitaxy. Cross-sectional TEM confirmed the epitaxial relationship between the films and the substrates. Double positioning boundaries have not been observed in the material grown on the 6H-SiC substrates. Platinum and Ti circular contacts were epitaxially deposited on α(6H)-SiC via electron beam MBE at room temperature. Leakage currents at –10V were as low as 5×10^{-18} A/cm^2. The ideality factors were approximately unity. Barrier heights for the as-grown Ti and Pt contacts were determined from C-V measurements to be 0.88 eV and 1.02 eV, respectively. Theoretical investigations of the physical limitations to the RF operation of SiC IMPATT diodes have shown that good RF output power can be obtained from these devices. However, the low magnitude of the charge carrier mobility in SiC limits the magnitude of the RF voltage that can be supported, and thereby prevents efficient dc to RF power conversion. MESFETs have been fabricated with values of f_t and f_{max} of 4.5 GHz and 3.0 GHz, respectively. The measured DC power density was extremely high with a value of 12.4 W/mm. Solutions to the problems of parasitics from source and gate resistances are described.

14. SUBJECT TERMS
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Table of Contents

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SUMMARY OF ALL WORK ACCOMPLISHED

I. Introduction

The SiC polytype that currently shows the most promise for high power microwave performance is 6H-SiC. The reason for this choice lies in the high quality and availability of this material more than in its basic electrical properties. For instance, an IMPATT diode relies on operation of a diode in avalanche; while very good avalanche characteristics can now be attained with pn junction diodes in 6H-SiC, no avalanche characteristics have been reported for β-SiC diodes. Likewise, no stable MESFET characteristics have been reported for β-SiC for drain voltages higher than 10 V, while 6H-SiC MESFETs are capable of withstanding considerable drain voltages (>100 V). The ability to operate at these higher fields is key to the success of SiC at high frequencies. Because of the excellent crystal quality of 6H-SiC currently being produced by Cree Research, devices fabricated from this material can operate reliably in these high fields.

In order to investigate the suitability of SiC for use in fabrication of high frequency electronic devices, various device types are being modeled in this research program. This investigation is expected to provide guidance regarding device structures most suitable for implementation in this material. Devices currently under consideration include the MESFET, IMPATT diode and Bipolar Transistor. These devices are commonly fabricated from Si and GaAs and are used at microwave and mm-wave frequencies. The material parameters of SiC indicate that this material may allow devices with improved performance to be fabricated. Devices with improved RF output power, in particular, are very likely in SiC.

To achieve the aforementioned devices, as well as other device structures, such that they are operable at or near their theoretical capacity, it will be necessary to improve the ohmic and Schottky contacts to the material and to understand the fundamental science underlying the nature of the interface and its relationship to the electrical properties. A limiting factor in improving performance of SiC based devices is the ability to control the electrical characteristics of metal/SiC contacts. An ohmic contact, characterized by a low contact resistance and a linear current-voltage relationship, generally is more difficult to obtain due to the need to effectively eliminate any barrier to electron transport. For good rectification properties a large potential barrier between the metal and the semiconductor is desired.

As the above challenges to the advancement of the existing technological base of electronic SiC are being investigated, it is necessary to advance the state-of-the-art, especially in the area of low temperature growth of more perfect thin films. To this end a

molecular beam/atomic layer epitaxy (MBE/ALE) system for growth of SiC films by the technique of gas-source molecular beam epitaxy has been designed, fabricated and commissioned for this purpose during the course of this contract.

The principal objectives of this contract have been the modeling, fabrication and characterization of SiC-based microelectronic devices for microwave applications, the development and characterization of rectifying contacts for n-type SiC and molecular beam deposition equipment development and utilization for the growth of ultra-high purity thin films of SiC at lower temperatures than employed for chemical vapor deposition. The procedures, results and discussions of these results are presented in the following sections. Each of these sections is self-contained with its own figures, tables and references.

II. Growth and Characterization of β-SiC Films on Si and 6H-SiC by Gas-Source Molecular Beam Epitaxy

1. Introduction

At present, economics and availability make Si and a two-step chemical vapor deposition (CVD) the most commonly used substrate and process route for the growth of SiC films. However, mismatches in lattice parameters and coefficients of thermal expansion of 20% and 8%, respectively, exist between the two materials. The CVD process involves the reaction of the Si substrate surface with a C-containing gaseous species to form a "converted" layer of β-Si [1] prior to subsequent deposition of the β-SiC film using both C- and Si-containing precursors.

However, the high growth temperatures and level of control of growth parameters and doping species obtained with CVD have sparked interest in the technique of gas-source molecular beam epitaxy (GSMBE) for growth of SiC [2-4]. The latter technique allows for precise control of growth parameters and minimization of sample contamination during deposition and was used in the studies described below. Experiments were conducted to determine the feasibility of SiC growth directly on Si (100) and to offer a comparison to films to be grown on converted layers in the near future. Effects of the C_2H_4/Si_2H_6 ratio and growth temperature on film morphology and quality were examined.

2. Experimental Procedures

Growth System. A schematic of the system to be used for gas-source MBE is shown in Figure 1. Samples are introduced into a small load lock chamber, the chamber is evacuated, and the samples are transferred to the heating stage in the growth chamber. The load lock is pumped by a Balzers TPU 060 turbomolecular pump backed by a Sargent-Welch rotary vane pump. Pressures of 1×10^{-6} torr or below are easily reached in 30 minutes, at which point samples are transferred to the growth chamber.

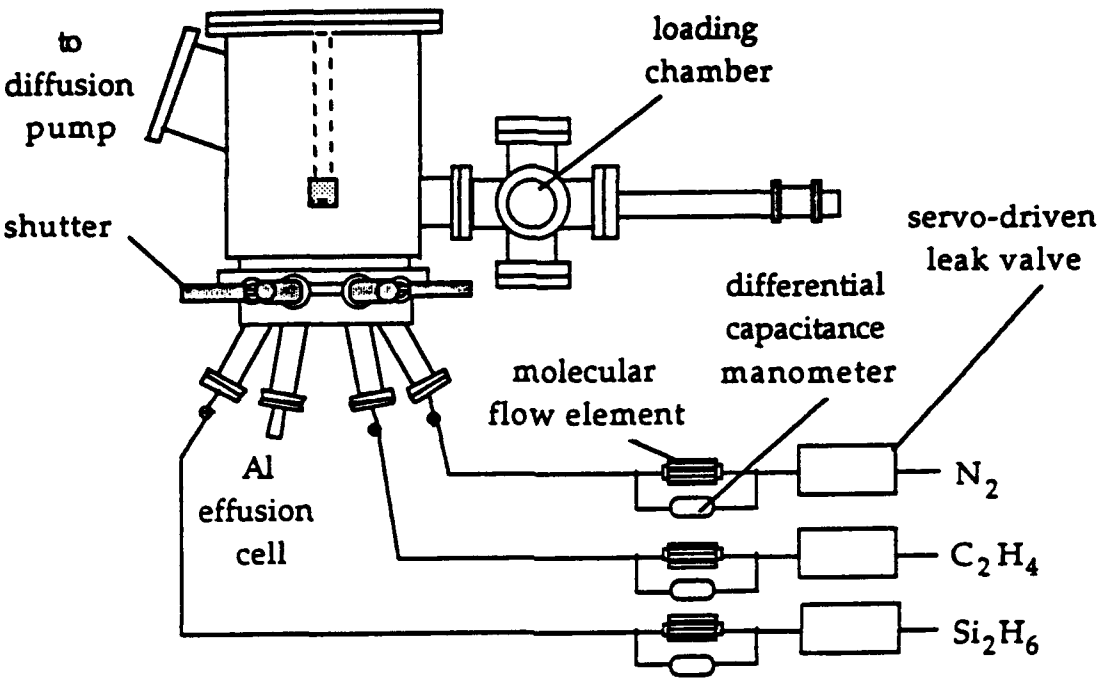


Figure 1. Schematic of molecular beam epitaxy apparatus.

Samples are heated using a specially designed heater composed of a coiled tungsten filament contained within a SiC-coated graphite cylindrical heating cavity lined with molybdenum and tungsten radiation shielding. A high-purity pyrolitic BN disk is used as an insulating plate for holding the W coil in place. The sample is shielded from line-of-sight interactions from all parts of the heater not coated with SiC to minimize sample contamination. The heater is capable of temperatures of over 1000°C. Samples can also be rotated during growth to ensure sample uniformity.

Species used in growth are introduced by way of the source flange. The source flange is equipped with ports for up to five solid sources and five gaseous sources. Disilane (Si_2H_6) is currently used as the source of silicon and is supplied through a pressure-controlled flow system involving a pressure gauge (baratron) and a flow element. Ethylene (C_2H_4) is currently used as the source of carbon. It is presently introduced in the same manner as the disilane. However, it is planned to decompose it in an Ar^+ plasma downstream from a specially designed ECR plasma source. The p-type dopant of aluminum is provided by a solid-source MBE effusion cell. Diatomic nitrogen (N_2) decomposed with an ECR source is used as source of nitrogen which is the n-type dopant. Mechanical air-actuated shutters are used with all sources to aid rapid switching between sources for abrupt doping profiles.

Growth of β-SiC (100) on Si (100) Substrates. Growth experiments were conducted using Si substrates primarily cut 4° off (100) toward the [011] direction. The use of off-axis substrates eliminates inversion domain boundaries (IDB's) [5,6]. The chemically cleaned (5 min. H_2SO_4 (60°C), 1 min DI rinse, 5 min 1:1 H_2O_2/NH_4OH (60°C), 1 min DI rinse, 5 min BOE, 1 min DI rinse) substrates were introduced into the growth chamber shown in Figure 1 and resistively heated for 180 s at the growth temperature to desorb the native oxide layer.

Growth conditions used in this study were as follows: temperature, 1298-1498 K; pressure, $4\text{-}6\times10^{-5}$ torr; Si_2H_6 flow rate, 0.40-2.0 sccm; C_2H_4 flow rate, 2.0 sccm; and time, 90 min. The resulting films were 30-50 nm in thickness. The chemical composition and depth profile of each sample were obtained using a scanning Auger microprobe. Samples which showed a 1:1 Si to C ratio from the Auger results were examined using an optical microscope and a field-emission scanning electron microscope (SEM) to observe surface morphology. Reflection high-energy electron diffraction (RHEED) was used after growth was completed to determine the crystalline quality of the SiC surface. Cross-sectional transmission electron microscopy (XTEM) also was employed to analyze representative β-SiC films.

Growth of Al-doped β-SiC on 6H-SiC. These films were grown on the Si face of 6H-SiC (0001) substrates provided by Cree Research, Inc. The substrates were nominally on-axis (± 1° off (0001)), as determined by X-ray diffraction using the Laue back-reflection method. The material sources were also the gases of Si_2H_6 for silicon, C_2H_4 for carbon and solid Al for the p-type dopant. The last material was evaporated from a standard Knudsen-cell. The 6H-SiC substrates were chemically cleaned prior to growth using a BOE etch at room temperature for 5 min, followed by a DI water rinse for 2 min. This limited cleaning process was used to preserve a sputtered carbon layer present on the back of the wafer as an aid in temperature measurement.

In order to desorb hydrocarbon and oxide layers from the SiC surface, the sample was heated under vacuum to 1250°C for 5 min prior to growth. An Al-doped layer of β-SiC was formed by GSMBE on the converted layer using these conditions: Si_2H_6 flow, 0.5 sccm; C_2H_4 flow, 1.0 sccm; sample temperature, 1250°C; Al source temperature, 960°C; and time, 100 min. The system base pressure was less than 1×10^{-9} torr; pressures during the SiC GSMBE growth typically reached 3×10^{-5} torr.

The surface morphology of the resultant films was examined using optical microscopy and field-emission scanning electron microscopy (SEM). The change of atomic concentration of Al vs. depth was determined using secondary ion mass spectrometry (SIMS). A Cameca IMS-3f ion microprobe was used for this purpose. Mass-filtered O_2^+ at 50 keV was used as the primary ion with a beam raster size of 250 μm. The atomic concentration of Al at each point in the SIMS profile was obtained by multiplying a

conversion factor by the value of the Al/Si count ratio at that point. The conversion factor was determined from the product of the Al/Si count ratio of an Al-implanted profile standard and the theoretically calculated atomic concentration at the peak of this standard. High-resolution transmission electron microscopy (HRTEM) was employed to determine the defects and crystalline structure present in the film as well as examining the film/interface region. An Akashi EM-002B HRTEM was used for this purpose.

C. Results and Discussion

Growth of β-SiC (100) on Si (100). Auger spectra from the surface of each sample showed the presence of an oxide from atmospheric exposure between growth and analysis. However, the underlying films in most samples were stoichiometric SiC. Figure 2 shows the Auger depth profile adjusted for differences in Auger yield of Si and C from a sample grown directly on off-axis (100) Si at 1298K using 2.0 sccm C_2H_4 and 0.4 sccm Si_2H_6 for 90 min. The results indicate essentially a 1:1 SiC ratio. The oxygen profile within the film is representative of the background level for this Auger system. A monocrystalline β-SiC film previously grown in our laboratory on (100) Si using CVD showed a depth profile nearly identical to that found in the SiC film shown in the figure. Figure 3(a) shows the RHEED pattern ([110] beam azimuth) of the same sample used to obtain the Auger profile of Fig. 2. The RHEED pattern of a sample grown for 90 min on off-axis (100) Si at 1248 K with 2.0 sccm C_2H_4 and 1.0 sccm Si_2H_6 is shown in Fig 3(b). Both samples were monocrystalline β-SiC and were of similar crystalline quality. Twin spots were detected in the RHEED micrographs.

Auger results indicated that only certain C_2H_4:Si_2H_6 flow ratio and temperature combinations resulted in growth of single phase SiC. For example, Si-rich films were obtained for 2.0 sccm C_2H_4 and 0.4 sccm Si_2H_6 at 1248 K and at 1348 K. However, at 1298 K, the film grown using these flow rates was stoichiometric SiC. Films grown using 2.0 sccm C_2H_4 and 2.0 sccm Si_2H_6 were also Si-rich at 1348 K, but were stoichometric at 1298 and 1248 K. Films grown using 2.0 sccm C_2H_4 and 1.0 sccm Si_2H_6 were nominally 1:1 SiC over the entire temperature range investigated. The reasons for these variations are being studied.

Transmission electron microscopy (TEM) was used to evaluate the structural quality of the films. Figure 4 shows a high-resolution cross-sectional micrograph and corresponding (110) electron diffraction patterns of both the β-SiC film grown at 1298 K for 90 min and the Si substrate. Both the SiC/Si interface and the SiC surface were fairly rough. The region at the substrate/film interface appears to be amorphous in the micrograph; this is believed to be caused by damage from the ion milling used as part of the TEM sample preparation procedure. A high concentration of defects, namely [111] microtwins and

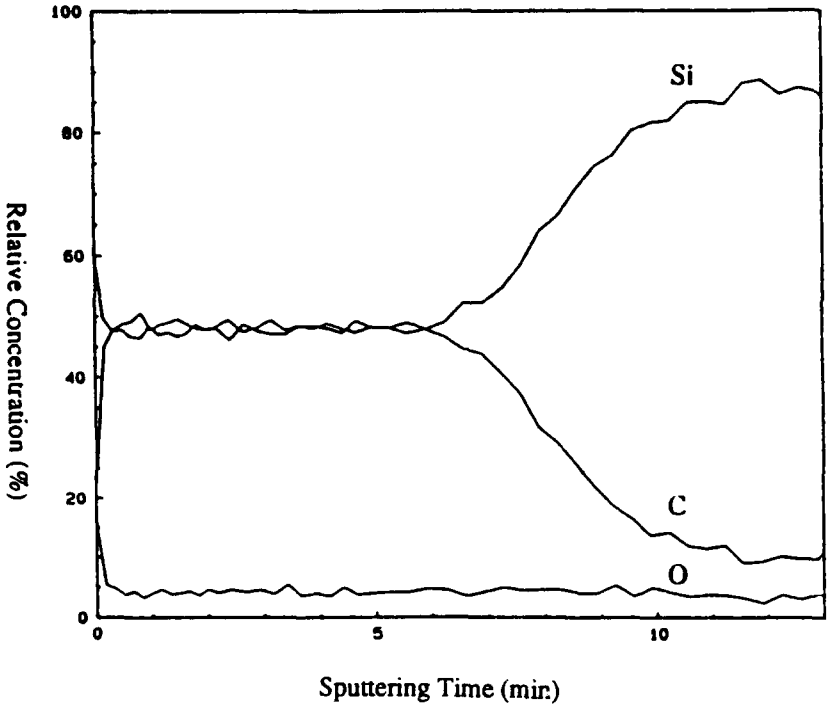
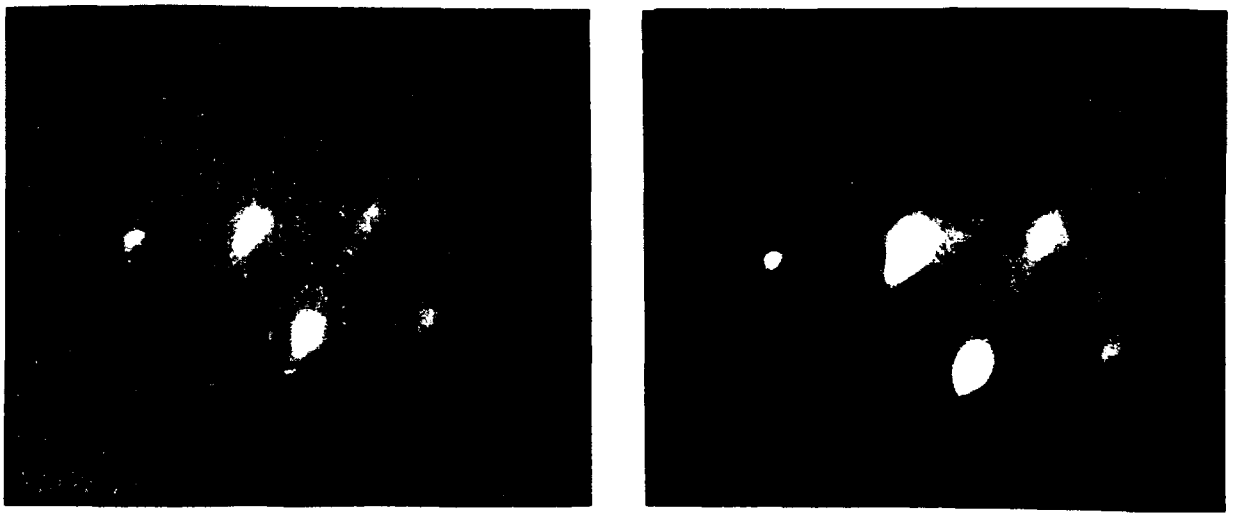


Figure 2. Auger depth profile of sample grown at 1075°C.



a) 1075°C, C/Si: 5:1

b) 975°C, C/Si: 2:1

Figure 3. Rheed of β-SiC films on Si (100) substrates.

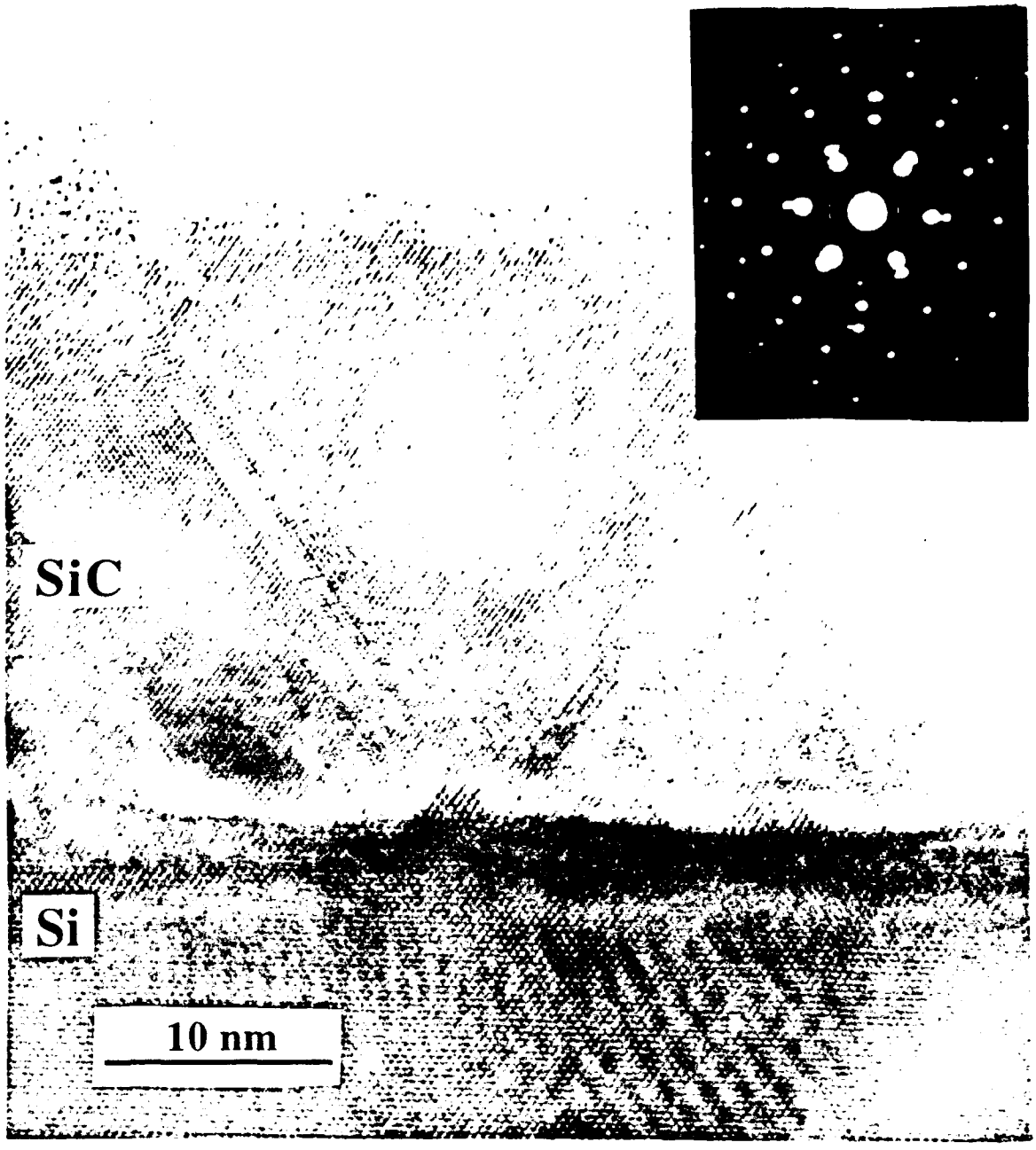


Figure 4. Cross-sectional TEM micrograph of SiC/Si sample grown at 1075° with inset of selected area diffraction pattern of the SiC film and Si (100) substrate.

misfit dislocations, are readily visible in the SiC film in the figure. An epitaxial relationship between the SiC films and the Si substrate can clearly be seen in the figure.

Growth thicknesses were estimated from Auger depth profiles and correlated with thicknesses obtained for samples examined using XTEM. The average values were 30-50 nm for 90 min of growth.

Growth of Al-doped β-SiC on 6H-SiC. An SEM micrograph of a heavily Al-doped film grown on SiC (0001) is shown in Figure 5. The surface of the film is fairly smooth, though the existence of small platelets on the surface can be seen as areas of lighter contrast in the micrograph. In the research reported by other investigators [7], optical microscopy normally has revealed a mosaic structure consisting of what appeared to be steps and ledges on the β-SiC film on the α-SiC substrate. However, an examination of the film grown in the present research using Nomarski optical microscopy found only occasional areas with this mosaic pattern. The steps and ledges typically seen result from double positioning boundaries, which result when two adjacent β-SiC (111) nuclei form rotated 60° to each other about the <111> axis [8]. Over the bulk of this film, very few of these DPBs could be found using Nomarski optical microscopy or SEM. It is unclear whether the lack of appearance of DPBs is due to the fact that the film is quite thin (100 nm) or that the nuclei are very small, or the presence of Al has a positive effect or that low temperature MBE growth is effective in eliminating these defects. Plan view TEM and X-ray topography has been used in the past to elucidate these defects, and these techniques will be attempted to determine the presence of DPBs.

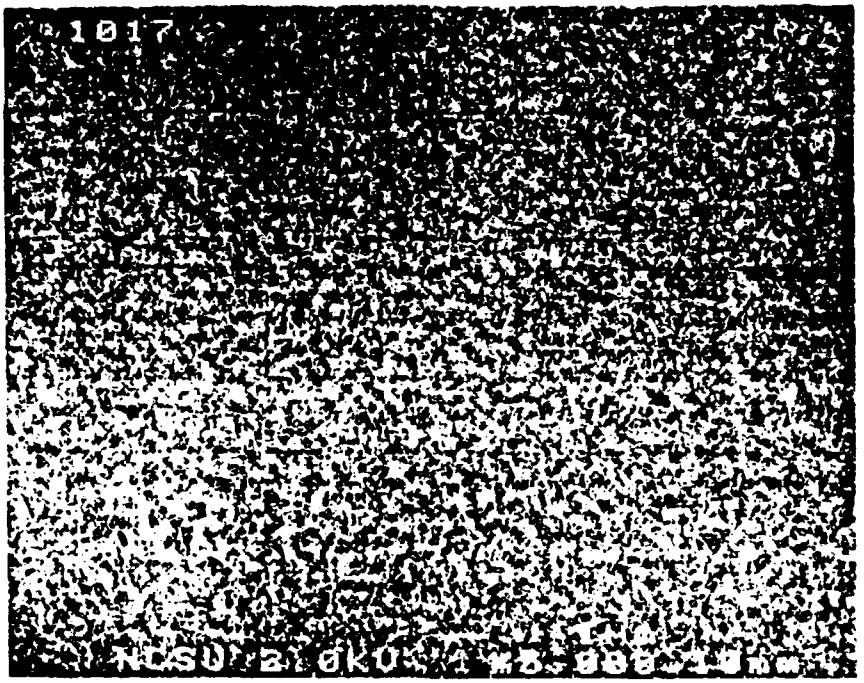


Figure 5: Scanning electron microscopy micrograph of the surface morphology of a heavily Al-doped β-SiC film by scanning electron microscopy.

A plot of Al atomic concentration vs. depth for this sample is shown in Figure 6. The substrate should have a much lower concentration of Al than the film which was intentionally heavily doped. The peak concentration of Al is high (5×10^{20} cm^{-3}). However,

the Al concentration drops rapidly with depth. It is believed that the small hump seen at a sample depth of about 100 nm denotes the interface between the β-SiC film and the 6H-SiC substrate. There should be some small amount of strain at this interface (even though the substrate and film are both SiC). This strain is primarily due to the different doping levels and impurity concentrations of the film from the substrate, and also the different crystal structures of the two SiC polytypes. This interfacial strain energy, though small, would enable the formation of lower-energy sites for impurity species such as Al. This decrease in lattice strain energy resulting from the incorporation of Al near the interface would encourage migration of this species to the interface during deposition.

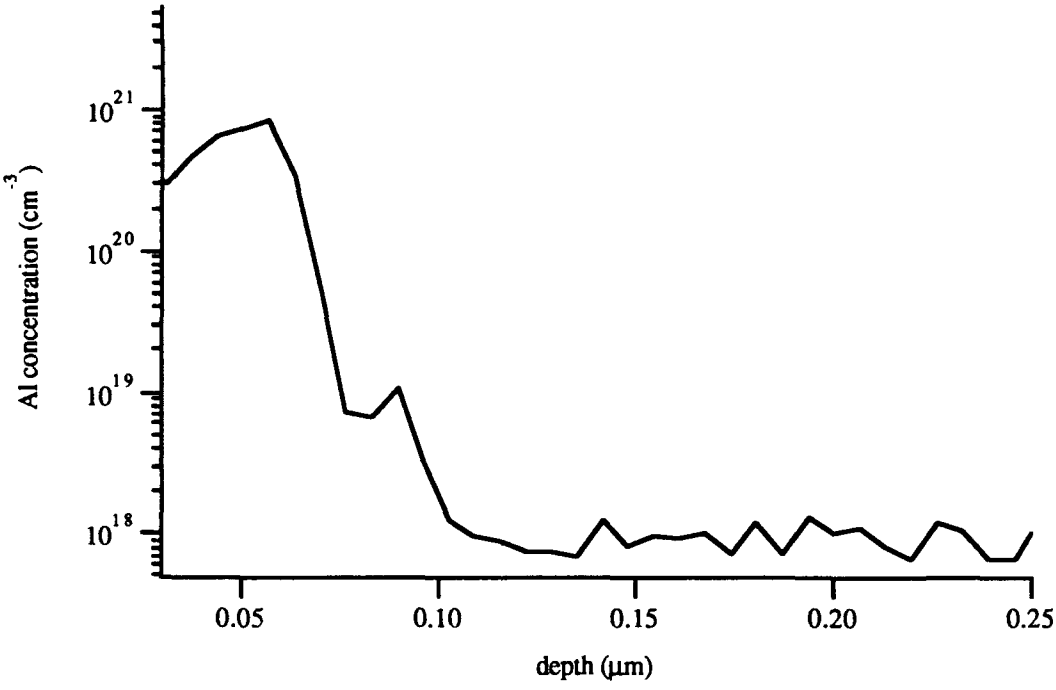


Figure 6. Atomic concentration vs. depth of Al in β-SiC film deposited on α(6H)-SiC substrate.

Figure 7 is a cross-sectional HRTEM micrograph of a portion of the film and the β-SiC/6H-SiC interface. The substrate is oriented so that the [11$\bar{2}$0] direction of the 6H-SiC substrate is perpendicular to the plane of the image. It was deduced that the 6H-SiC substrate used in this experiment was almost exactly in the (0001) orientation due to the lack of steps at the top of the 6H-SiC substrate layer. From the lattice images of the film, the grown layer is deduced to be cubic and in the (111) orientation. Several (111) stacking faults can be seen in the micrograph (where the film appears to become 6H-SiC for a few layers). A selected area diffraction (SAD) pattern of the film and the substrate is shown in Figure 8. Diffraction spots from both the 6H-SiC substrate and the β-SiC layer can be

seen. The epitaxial relationship between the substrate and the β-SiC film can also be observed both from the micrograph and the corresponding SAD pattern.

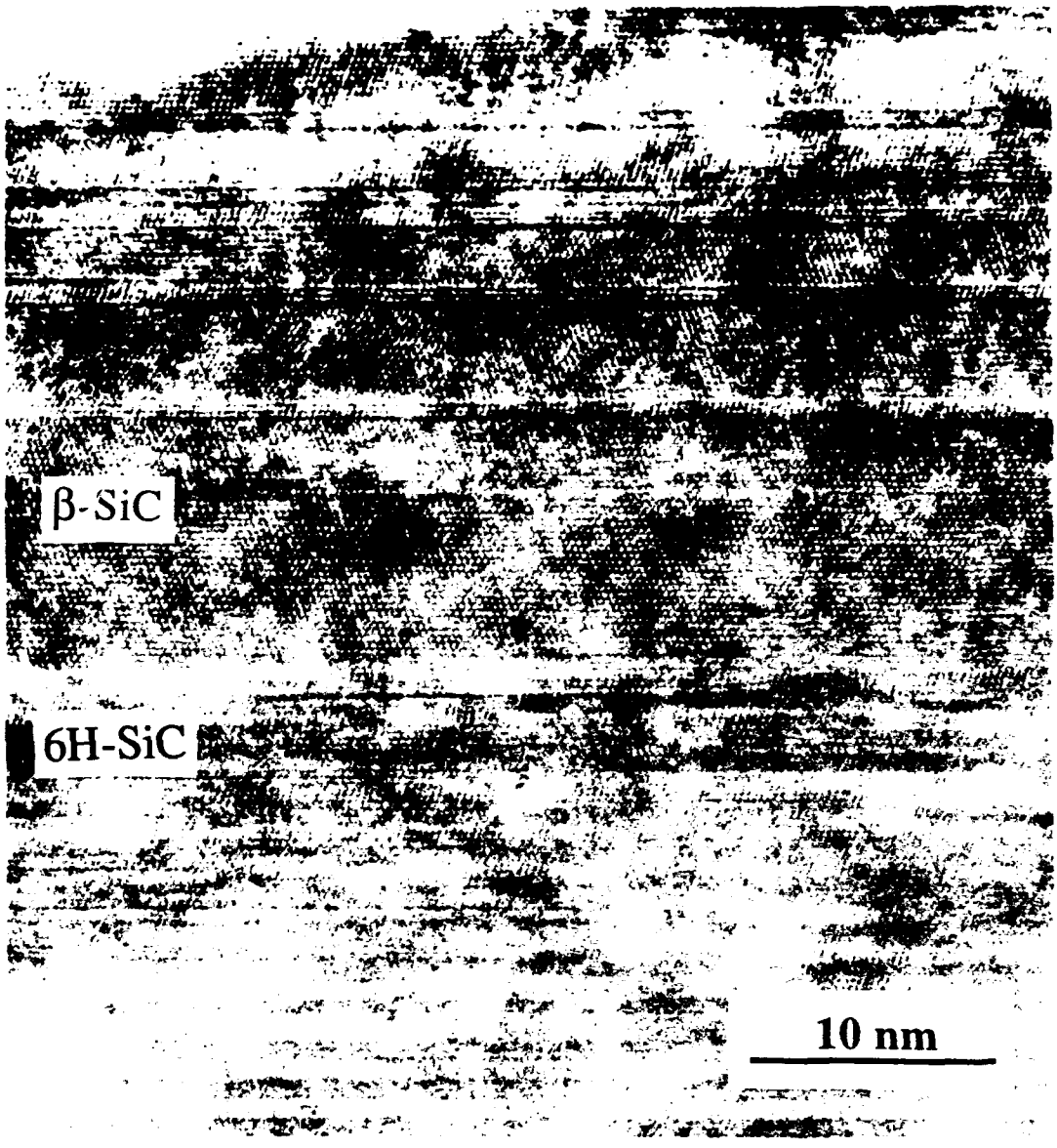


Figure 7. Cross-sectional HRTEM image of β-SiC film and 6H-SiC substrate.

The surface morphology of the as-grown film is fairly smooth, and appears to be relatively free of DPBs, as compared to conventional CVD growth. Several researchers [9-13] have suggested that variations in surface treatment prior to growth can change the density of or virtually eliminate DPBs formed on the resultant film. Variations in cleaning method have been shown to change DPB density, with the lowest DPB density obtained on the as-received wafers in one study [12]. The effects of annealing in H_2 and growth of thin Si and C layers prior to β-SiC growth on 6H-SiC substrates have also been examined, with

most promising results obtained using conversion of a Si pre-growth layer to SiC followed by SiC film growth [13]. In any case, pre-growth treatment of the substrate has been shown to affect DPB density. It is conceivable that DPB formation could be arrested using MBE, if the initial several layers formed were somehow continuous. The level of control using MBE is much greater than with CVD, and this greater control could allow for layer growth on 6H-SiC substrates. Examining the films during growth using *in situ* reflection high-energy electron diffraction (RHEED), as is planned in the near future, should prove conclusive as far as determining whether layer growth is present in the first few monolayers of β-SiC. In addition, as mentioned previously, examination of the MBE-grown films using other methods such as plan-view TEM is necessary to determine whether DPBs actually are present.

Figure 8. Selected area diffraction pattern of β-SiC film and 6H-SiC substrate.

The β-SiC film discussed in this report is heavily doped with Al, with a peak concentration of 7×10^{20} cm^{-3}. A value of concentration this high is suspect, and as a result, attempts to duplicate this result are in process. I-V characteristics taken without a rectifying contact indicate that this sample is p-type. Electrical measurements (I-V and C-V) on this sample are being conducted in order to determine both carrier concentration in the layer as well as characterize the p-type β-SiC/n-type 6H-SiC p-n junction. A high concentration of Al may help to explain the presence of <111> stacking faults seen in Figure 9. The concentration of Al in this film, if the SIMS data is correct, would produce large amounts of strain in the film because of the larger size of the Al atom in a tetrahedral bonding configuration. This strain could induce the formation of these stacking faults as a way of

alleviating it. Double crystal X-ray diffraction could prove useful in determining the amount of strain present.

D. Conclusions

Monocrystalline β-SiC films were grown by GSMBE on off-axis Si (100) substrates using Si_2H_6 and C_2H_4 at temperatures as low as 1248 K. This temperature is much lower than that typically used for SiC CVD growth. Films appeared smooth and specular to the naked eye, but [111] pyramidal growth pits were present on the film surface. Preferential growth on the pit edges under certain growth conditions was also observed. Cross-sectional TEM analysis of selected SiC films showed the presence of [111] microtwins and visually confirmed the epitaxial relationship between the film and the Si substrate.

Gas source MBE growth of heavily Al-doped epitaxial layers of β-SiC (111) on 6H-SiC (0001) has also been achieved at 1250°C using C_2H_4 and Si_2H_6 as source gases. This growth temperature is 250°C lower than that typically used in CVD. High-resolution TEM showed a coherent interface between the film and substrate and the presence of [111] stacking faults. The latter occurred periodically in the β-SiC film. These stacking faults may prove to be due to strain induced by the large concentration of Al present in the film. Surface morphological examination of films using SEM and optical microscopy showed an apparent lack of DPB formation. Further characterization is necessary to determine whether or not DPBs exist in these films. SIMS analysis suggested the presence of a high concentration of Al in these films. Electrical measurements will be conducted in the future.

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III. DEPOSITION AND CHARACTERIZATION OF TITANIUM AND PLATINUM RECTIFYING CONTACTS ON N-TYPE ALPHA 6H-SiC

A. Introduction

A critical issue in current SiC device technology is the ability to choose metals which are good ohmic and rectifying contacts stable at high temperatures. This issue is in turn dependent upon the ability to create a clean surface, to unpin the Fermi level in the semiconductor, and to identify any changes in phase which occur as the temperature is raised.

And therefore, it is an interplay between science and technology which is critically necessary for both long and short term advancement of the quality of contacts.

For an ideal, abrupt junction (at which thermionic emission over the barrier holds) the barrier height is defined by the Schottky-Mott limit, or the difference between the metal work function and the electron affinity of the semiconductor. However, interface states between the metal and semiconductor and traps common to wide bandgap semiconductors cause deviations from ideality. In fact, Pelletier *et al.* [1] have reported Fermi level pinning in 6H-SiC due to intrinsic surface states, indicating little dependence of barrier height on the work function of the metal. On the other hand, Waldrop *et al.* [2] have reported strong work function dependence for metal/β-SiC barrier heights, giving encouragement for the ability to control barrier heights of metals on 6H-SiC.

This report describes the characteristics of Ti and Pt contacts (which were chosen based on their work functions and physical properties) to n-type 6H-SiC. Because Pt has one of the largest work functions of all pure metals, a large barrier Schottky contact is predicted for an ideal junction The merits for Ti/SiC contacts include the similar crystal structures of Ti and 6H-SiC and knowledge of phase formation from previous studies of Ti/SiC diffusion couples [3]. The identification of phases as a function of annealing provides a foundation for understanding the electrical characteristics as the chemistry of the metal-SiC contact changes.

Not only is the particular choice of metal important, but the processing also plays a critical role. More specifically, the nature of the substrate surface, in terms of contaminants, depends on the processing techniques and can control the contact characteristics. This report describes the surface preparation procedure used to produce a 'clean' SiC surface, as well as the results of chemical analysis of the surface at key steps in the cleaning process, the deposition procedures and the results of electrical measurements of the characteristics of the contacts.

B. Experimental Procedure

Vicinal single crystal, nitrogen-doped, n-type ($10^{16} - 10^{18}$ cm^{-3}) substrates of 6H-SiC (0001) containing 0.5-0.8 μm thick, nitrogen-doped ($10^{16} - 10^{17}$ cm^{-3}) homoepitaxial films

were provided by Cree Research, Inc. The Si-terminated (0001) surface, tilted 3°-4° towards [1$1\bar{2}0$] was used for all depositions and analyses.

Prior to the deposition of the Ti contacts, the SiC substrates were cleaned using a sequence which involved a a 10 min. dip in an ethanol / hydrofluoric acid / deionized water (10:1:1) solution and a thermal desorption in ultra-high vacuum (UHV) (1–5 $\times$ 10^{-10} Torr). All processing steps were the same for the Pt contacts, except that a 10% solution of HF in deionized water was substituted for the wet chemical clean. A resistive graphite heater was used to heat the substrates at 700°C for 15 min. X-ray photoelectron spectroscopy (XPS) and low energy electron diffraction (LEED), both accessible by UHV transfer from the heating station and deposition chamber, were used to monitor surface chemistry and structure, respectively. The XPS system consisted of a Riber Mac2 semi-dispersive electron energy analyzer and a Riber pulse counter. The LEED studies were conducted using a Physical Electronics Instruments 11-020 electron gun. The metals were deposited onto unheated substrates by electron beam evaporation (base pressure < 2 $\times$ 10^{-10} Torr). The first 10 nm were deposited at a rate of 1 nm/min. The deposition rate was then increased to 2 – 3 nm/min. to give a total thickness of 100 nm. For electrical characterization, vertical contact structures consisting of 500 μm and 750 μm diameter circular contacts were created by depositing the metal through a Mo mask in contact with the (0001) SiC epitaxial layer, leaving a patterned metal film. Conductive liquid Ag served as the large area back contact. All subsequent annealing was done in UHV. Current-voltage (I-V) measurements were taken with a Rucker & Kolls Model 260 probe station in conjunction with an HP 4145A Semiconductor Parameter Analyzer.

Capacitance-voltage (C-V) measurements were taken with a Keithley Model 5956 Package 82 Simultaneous CV System in conjunction with an HP vector PC-308. The contact structures were the same as above. Measurements were taken at a frequency of 1 MHz.

Ti/SiC samples were prepared in cross-section for TEM analysis. High resolution images and selected area diffraction patterns were obtained with an ISI EM 002B operating at 200 kV.

C. Results

1. SiC Surface

The surface chemistry and structure of substrates after surface preparation were monitored with XPS and LEED, respectively. After chemically cleaning the substrates in a solution of ethanol, HF, and deionized water for 10 min., XPS results showed a Si 2p peak at approximately 101 eV, indicative of Si to C bonding in SiC [4-6]. No Si-O bonding which has been reported at 102.1 - 102.5 eV [4], was detected in the signal. However, small amounts of O and F were detected Other than a shift attributed to sample charging, the Si

peak remained essentially the same after a 700°C desorption for 15 min. On the other hand, a C 1s peak at 285 eV present initially was removed after the desorption. This change indicates the desorption of adventitious C (i.e hydrocarbons), while the major peak remained at 283.5 eV, as expected for C to Si bonding in SiC [4-7].

2. Ti Contacts

Electrical characteristics of both as-deposited and annealed Ti contacts to n-type SiC (1×10^{16} cm^{-3}) were measured. Current-voltage characteristics of as-deposited Ti (curve (a) in Figure 1) were rectifying with typical leakage currents at –10 V of 6 nA (1×10^{-7} A/cm^2); however, values as low as 0.4 nA (9×10^{-8} A/cm^2) were observed. Hard breakdown was not observed to a voltage of –100 V; instead, the leakage current continuously increased, reaching 30 μA at –100V. This soft breakdown is thought to be due to sharp-edge effects from the contact geometries. After annealing in UHV for 20 min. at 700°C, the characteristics degraded (curve (b) in Figure 1). However, the characteristics improved again with each subsequent 20 min. anneal (curves (c) and (d) in Figure 1).

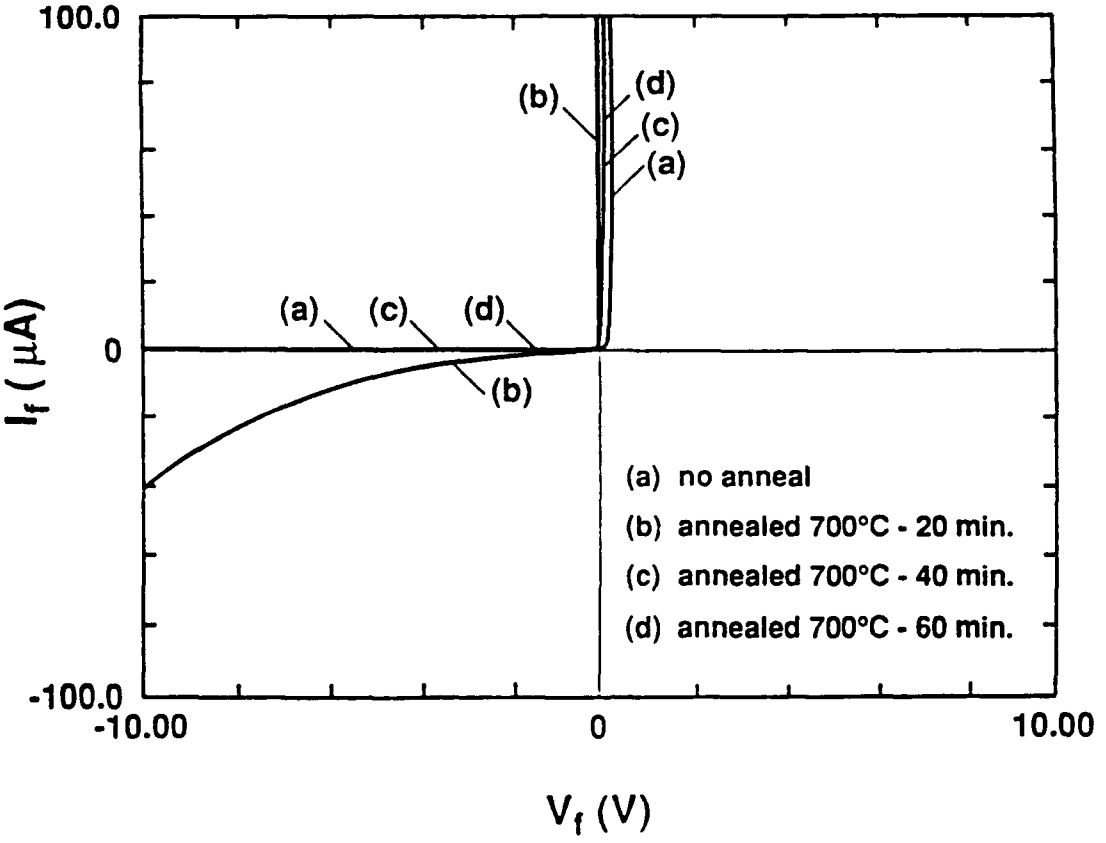

Figure 1. Current-voltage characteristics of Ti deposited on (0001) 6H-SiC epitaxial layer. (2.0×10^{-3} cm^2 contact area).

Notably low ideality factors for silicon carbide were calculated from plots of log I vs. V for all but the first anneal (Figure 2). For diodes in which the dominant current transport mechanism is thermionic emission and values of voltage V are greater than 3kT/q, the diode equation can be written as $J = Jo \exp(qV/nkT)$ [9], where J is the current density and n is defined as the ideality factor. Plots of log I vs. V showed linearity over 3 decades of current yielding values of n below 1.1. No ideality factor could be calculated for the first anneal as the linear regime was too small.

Although the calculated ideality factors are low, thermionic emission may not be the dominant current transport mechanism; therefore values for barrier height cannot be directly determined from current-voltage measurements (e.g. see Ref. [10]). Plots of log I vs. log V in the low voltage regime (Figure 3) indicate that current transport is probably dominated by space charge limited current (SCLC), a mechanism which frequently occurs in wide bandgap semiconductors [11].

On the other hand, barrier height values were calculated from differential capacitance measurements as a function of reverse voltage. A plot of $1/C^2$ vs. V should give a straight line such that

$$\Phi_B = V_I + \xi + kT/q \qquad (2)$$

where Φ_B is the barrier height, V_I is the extrapolated intercept at $1/C^2 = 0$, and ξ is the energy difference between the Fermi level and the bottom of the conduction band [9]. Figures 4 and 5 show $1/C^2$ vs. V plots for an as-deposited and an annealed Ti contact, respectively. These curves deviate slightly from linearity but appear to be linear over 1 – 2V. The deviation from linearity may be caused by series resistance and/or deep level traps in the bandgap of the semiconductor. By extrapolating the linear (low voltage) region of the curves, the voltage intercepts were found to be 0.67 V for the unannealed contact and 0.84 V for the annealed contact. For a doping level of 10^{16} cm^{-3}, these intercepts correspond to a barrier height of 0.88V for the as-deposited Ti/SiC and 1.04V for the annealed Ti/SiC.

Low energy electron diffraction, in which a diffraction pattern from the surface-region is obtained, was used to monitor the surface structure. The LEED pattern remained an ordered 1×1 after deposition of Ti and also through annealing to 900°C in 100°C increments for 10 min. at each temperature. Both Ti (a = 2.95 A, c = 4.68 A) and 6H-SiC (a = 3.08 A, c = 15.11 A) have hexagonal crystal structures, corresponding to a 4% lattice mismatch in the (0001) basal plane. The consistent 1×1 pattern of the SiC surface and these deposited Ti films indicates that growth has occurred epitaxially. Phase identification and structural analysis has been accomplished through collaboration with M.J. Kim and J.S. Bow at Arizona State

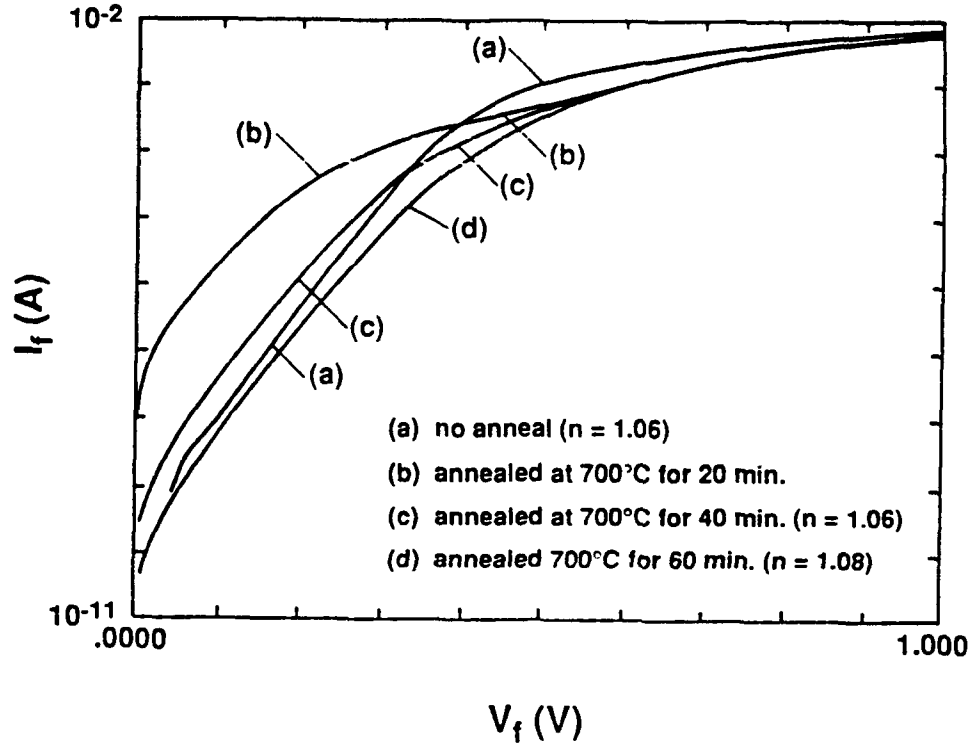

Figure 2. Log I vs. V of Ti deposited on (0001) 6H-SiC.

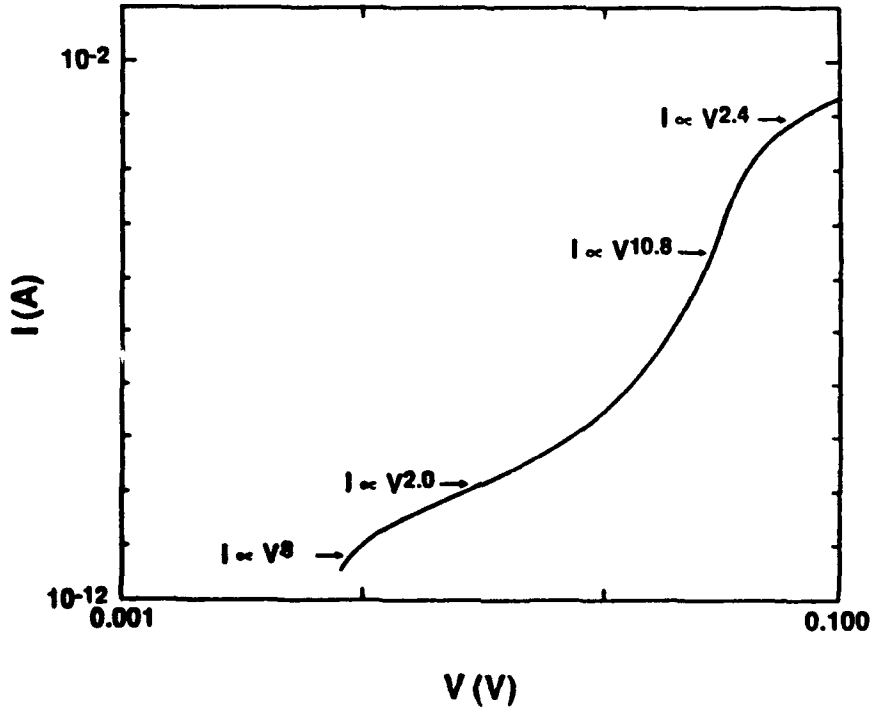

Figure 3. Log I vs. log V of as-deposited Ti/SiC.

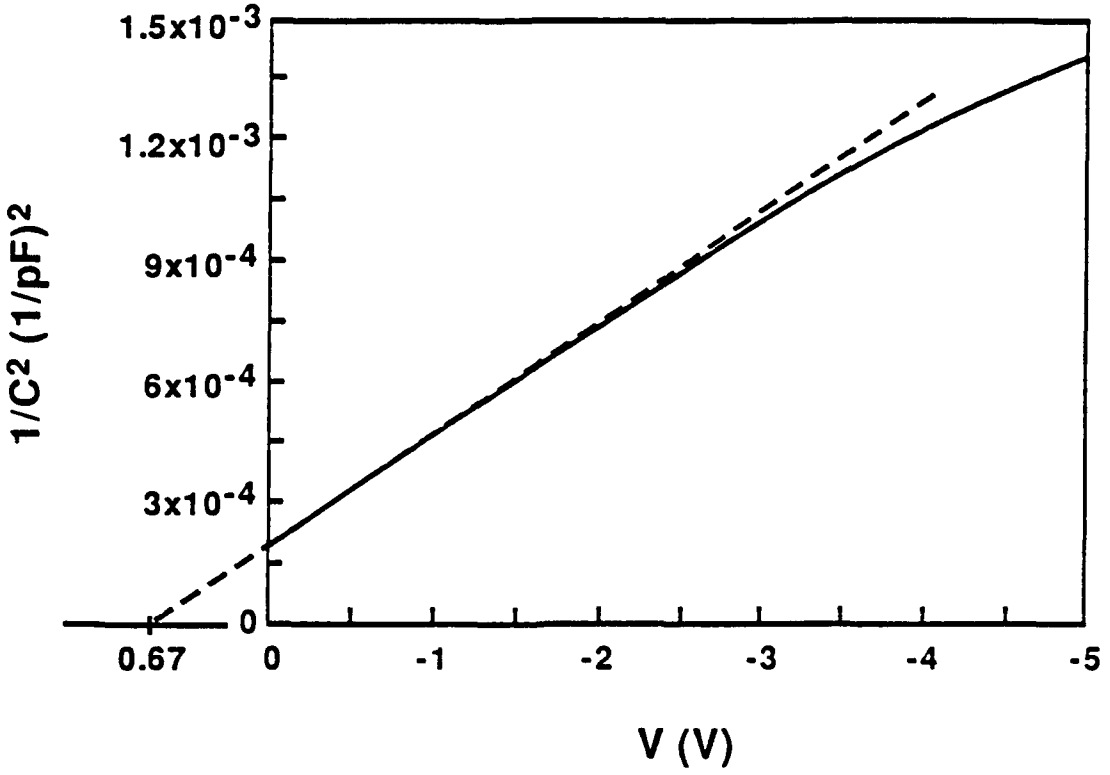

Figure 4. Differential capacitance-voltage measurements for as-deposited Ti/SiC plotted as $1/C^2$ vs. V. $\Phi_B \cong 0.88$ V.

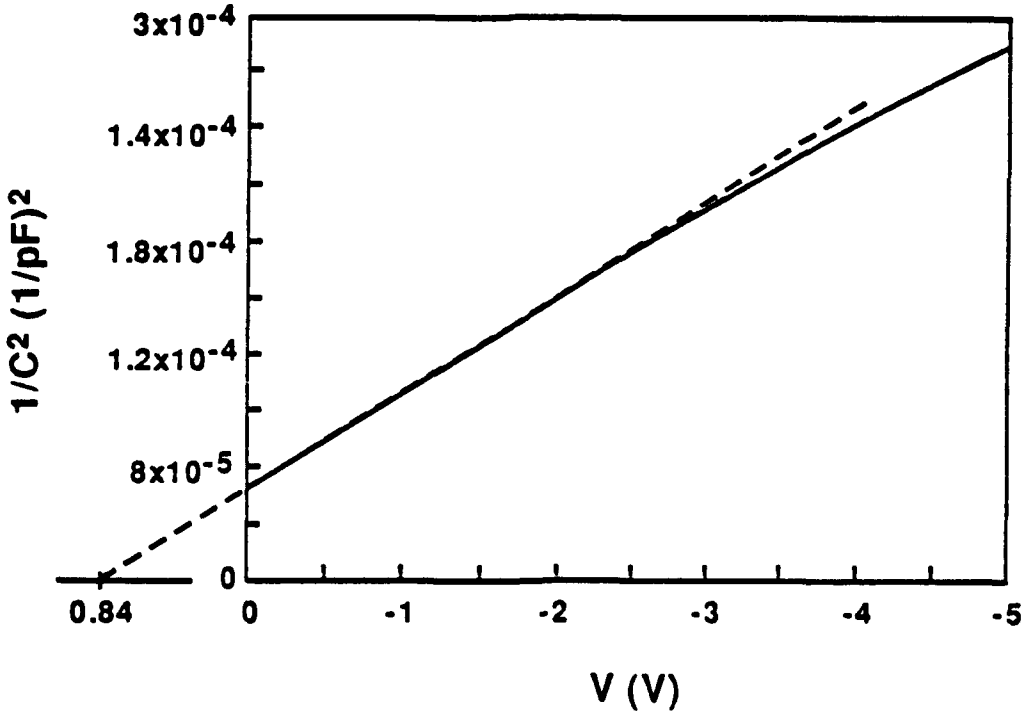

Figure 5. Differential capacitance voltage measurements for annealed (700°C for 60 min.) Ti/SiC plotted as $1/C^2$ vs. V. $\Phi_B \cong 1.04$ V.

University's Facility for High Resolution Microscopy. Figure 6 shows a high resolution image of titanium deposited on a bulk SiC (no epilayer) substrate at 400°C. The 6-layer periodicity in the SiC meets the 2-layer periodicity of the Ti at a non-atomically smooth interface. Close examination of the interface reveals that there appears to be regions of lattice matching. The strain resulting from the 4% lattice mismatch between the film and substrate is relieved by threading dislocations. Selected area diffraction patterns (Figure 7) show a superposition of the spot pattern for the film on that for the substrate, confirming the growth of single crystal titanium. For each orientation of the 6H-SiC [8], the Ti spots lie outside the SiC spots due to the smaller lattice parameter of Ti.

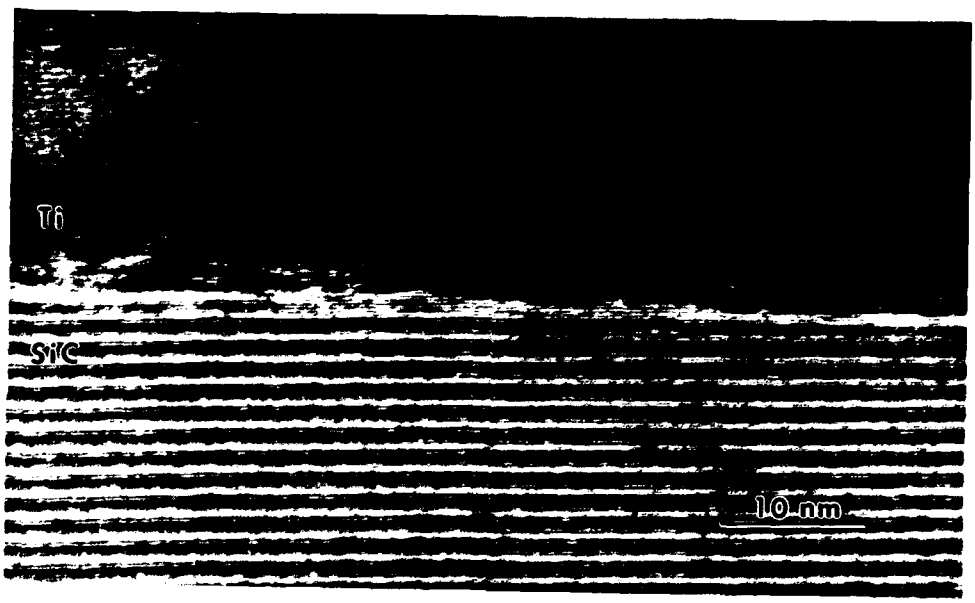

Figure 6. High resolution transmission electron micrograph of as-deposited Ti/SiC interface in cross-section. Ti deposited on (0001) SiC at 400°C.

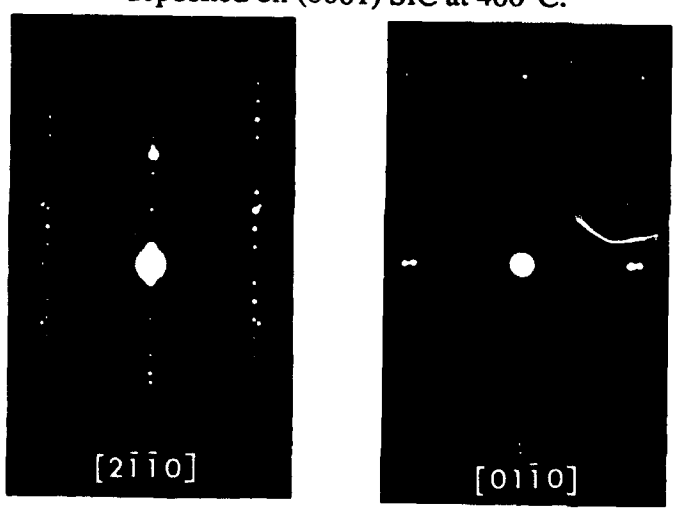

Figure 7. Selected area diffraction patterns of as-deposited Ti/SiC interface region in cross-section. Ti deposited on (0001) 6H-SiC at 400°C.

After depositing Ti onto a 6H-SiC epilayer at room temperature and annealing at 700°C for 20 minutes, a reacted layer approximately 20 nm thick has formed (Figure 8). Selected area diffraction patterns of the interface region (Figure 9) showed spots other than those seen for the as-deposited Ti/SiC interface. The 'extra' spots were identified as Ti_5Si_3 and TiC. The arrangement of these phases can be seen in Figure 10, which shows a magnification of the region marked "1" in Figure 8. A rather uniform layer of Ti_5Si_3 appears to form at the interface with SiC with particles of TiC at locations along the Ti/Ti_5Si_3 interface.

Figure 8. Cross-sectional high resolution TEM image of Ti/SiC reaction zone (annealed at 700°C for 20 minutes). Ti deposited on (0001) 6H-SiC at room temperature.

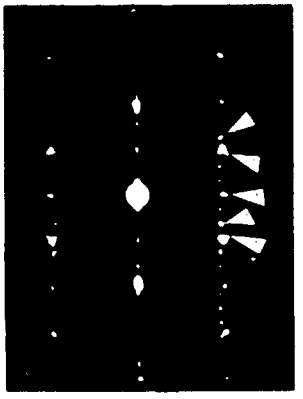

Figure 9. Selected area diffraction patterns of annealed (700°C for 20 min.) Ti/SiC interface region in cross-section. Ti deposited on (0001) 6H-SiC at room temperature. $z = [11\bar{2}0]_{SiC} = [11\bar{2}0]_{Ti} = [45\bar{1}0]_{Ti5Si3} = [011]_{TiC}$ "1" = Ti_5Si_3 "2" = TiC.

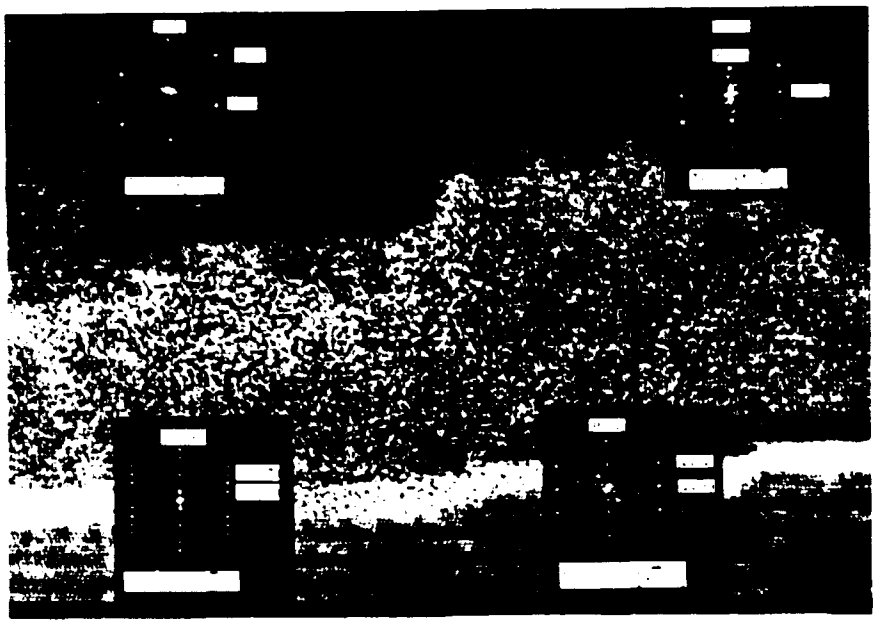

Figure 10. Magnification of the region marked "1" in Figure 8.

3. Pt Contacts

Current-voltage measurements of Pt contacts deposited on (0001) n-type SiC were also rectifying with typical leakage currents of 5×10^{-8} A/cm^2 at –10 V (Figure 11). The 'soft' breakdown observed is attributed to sharp edge effects due to the contact geometry and not to the material itself. However, it is the forward characteristics which give the most insight into the description of the contacts, and in particular the current transport mechanism.

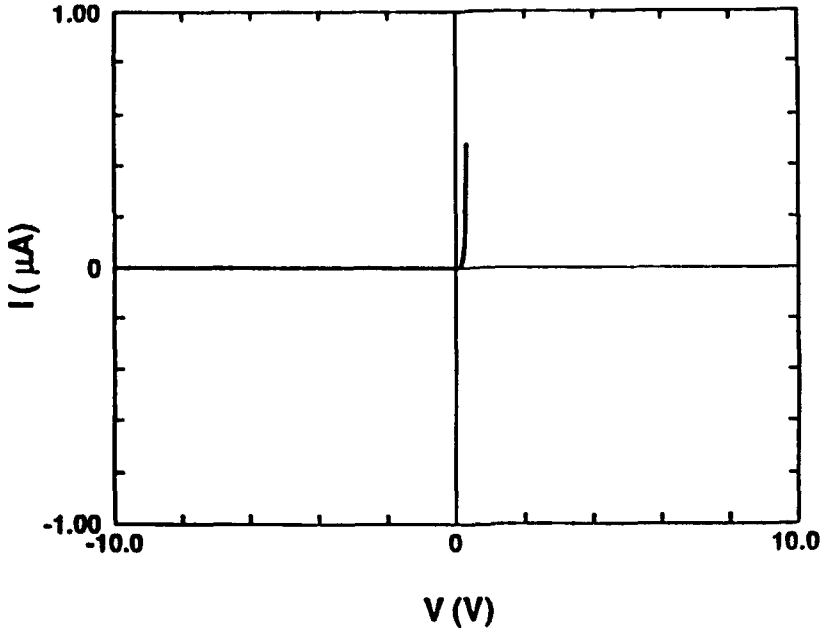

Figure 11. Current-voltage characteristics of Pt deposited on (0001) 6H-SiC epitaxial layer. (2.0×10^{-3} cm^2 contact area).

As was found for the Ti contacts, low ideality factors (1.02 – 1.08) were calculated for the Pt contacts (Figure 12). However, log I vs. log V plots are in contrast to those for Ti contacts. Figure 13 shows slopes much higher than a slope of 2, which is expected for space charge limited current [11]. The high slopes from the log I vs. log V plots in combination with the excellent log I vs. V characteristics suggest the possibility for thermionic emission controlled current.

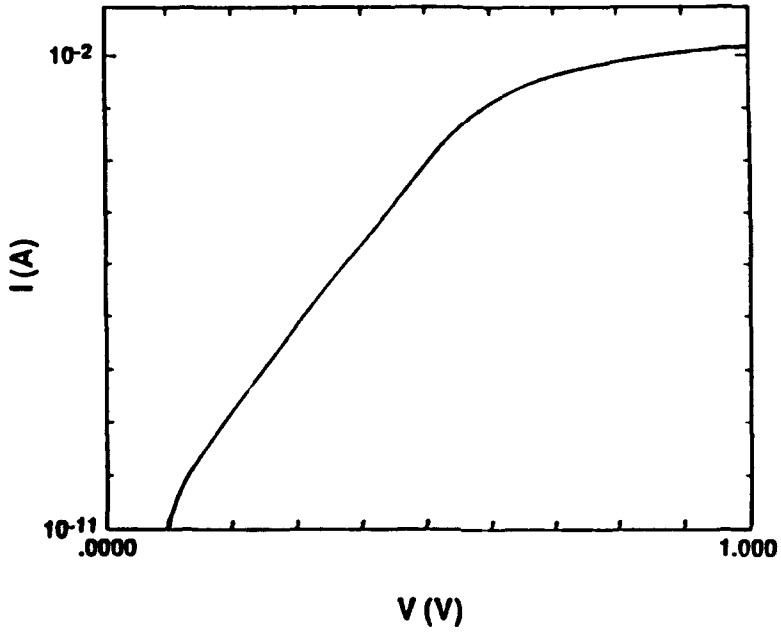

Figure 12. Log I vs. V of Pt deposited on (0001) 6H-SiC.

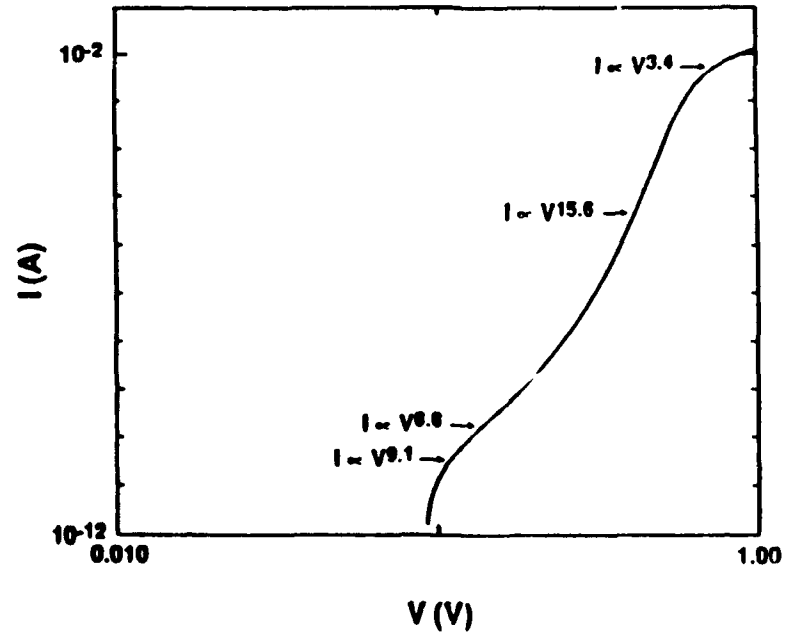

Figure 13. Log I vs. log V of as-deposited Pt/SiC.

A barrier height was estimated from capacitance – voltage measurements. A plot of $1/C^2$ vs. V shown in Figure 14 has an intercept on the voltage axis of 0.89 V. Again, the curve is linear over a 1-2 V range. For a doping level of 2×10^{17} cm^{-3}, this intercept corresponds to a barrier height of 1.02 V.

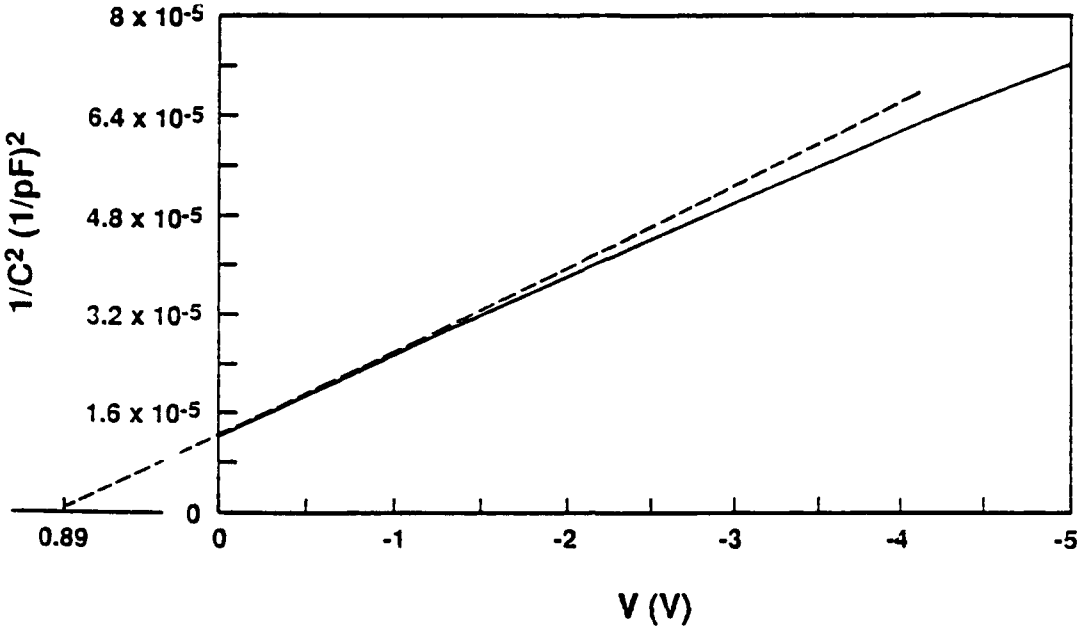

Figure 14. Differential capacitance-voltage measurements for as-deposited Pt/SiC plotted as $1/C^2$ vs. V. $\Phi_B \cong 1.02$ V.

D. Discussion

By subtracting the electron affinity of the semiconductor from the work function of the metal, theoretical, ideal barrier heights were calculated. Pelletier et. al. [1] have reported the Fermi level to be pinned near midgap in 6H-SiC with a work function of approximately 4.8 eV (intrinsic). Using a calculated value of 1.44 eV for the intrinsic Fermi level (measured from the the top of the valence band), the electron affinity (measured from the bottom of the conduction band to vacuum level) is estimated to be 3.38 eV. The work function of Ti is 4.33 eV, and that of Pt is 5.65 eV. From these work function values, barrier heights of 0.95 eV and 2.27 eV, respectively, are predicted. Although the 0.88 eV value calculated from C-V measurements for Ti (Figure 4) corresponds to a 7% difference from the predicted value of 0.95 eV, the calculated and predicted barrier heights for Pt correspond to a 55% difference. In addition, the measured barrier heights for the Ti and Pt contacts are within 0.14 eV of each other. It is obvious that more barrier height measurements are necessary before a conclusion can be drawn as to an accurate description of band bending and barrier heights.

The reaction chemistry on annealing directly affects the electrical characteristics (e.g. barrier height) because the characteristics become dependent upon the new interface formed with SiC. A reaction path in Ti/SiC diffusion couples at 1200°C in which TiC_{1-x} particles form in a matrix of Ti_5Si_3 has been reported [12] and is very similar to the results found in this study. However, some questions still remain in that the reported work function value of 3.71 eV for Ti_5Si_3 [13] would indicate a smaller barrier height of 0.33 eV. This prediction contradicts the experimental data (Fig. 8) in which a larger barrier height than that of the as-deposited Ti/SiC was calculated. With these issues in mind, more research on barrier heights and phase chemistry in the Ti/SiC system is anticipated.

The initial results from current-voltage measurements on Pt contacts give encouragement for taking elevated temperature measurements (and from these calculate Richardson's constant) and trying to determine barrier height. Not only were low ideality factors calculated from log I vs. V plots with a linear region of 5 decades of current, but log I vs. log V plots showed slopes which appear to be more indicative of thermionic emission than of space charge limited current. Comparison of Figures 2 and 12 shows that Pt has a sharper rise in current, which turns on at a higher voltage.

On the other hand, questions are raised from capacitance-voltage measurements. By extrapolating the low voltage region of the $1/C^2$ vs. V plot, a barrier height of 1.02 eV was calculated. This value is much lower than the 2.27 eV value predicted and close to the 0.88 eV calculated for as-deposited Ti. This may indicate that the Fermi level is pinned in the SiC due to surface states or traps in the bandgap. However, no conclusions can be drawn without further barrier height measurements and possibly measurement of traps by deep level transient spectroscopy (DLTS).

E. Conclusions

Both Pt and Ti contacts deposited on (0001) 6H-SiC at room temperature were rectifying with calculated ideality factors less than 1.1. While log I vs. log V plots of Ti contacts in the low voltage regime indicate that space charge limited current is the dominant transport mechanism, thermionic emission may hold for the Pt contacts.

Barrier heights were estimated from differential capacitance – voltage measurements. The measured value of 0.88 V for as-deposited Ti agrees quite well with the predicted value of 0.95 V. On the other hand, the increase in barrier height to 1.04 V for the annealed contact (700°C for 60 minutes) contradicts the decrease in barrier height predicted for the phases identified at the interface. After annealing for 20 minutes at 700°C, the interface has been found to consist of Ti_5Si_3 with particles of TiC.

Pt showed little variation from Ti in its barrier height measurements. The calculated value of 1.02 V is 55% smaller than the 2.27 V barrier calculated for the ideal case. The initial

measurements on Pt seem to indicate that there is little or no correlation between the barrier height and the work function of the metal.

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IV. Modeling and Characterization of Electronic Devices Fabricated from SiC—*6H-SiC IMPATT Performance and Limitations**

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Abstract

The physical limitations to the RF operation of IMPATT diodes resulting from the low magnitude of the charge carrier mobility in SiC are investigated by means of a numerical device model. The results of this investigation indicate that good RF output power can be obtained from SiC IMPATTs. However, the low magnitude of the charge carrier mobility in SiC limits the magnitude of the RF voltage that can be supported, and thereby prevents efficient dc to RF power conversion.

A. Introduction

Considerable interest has developed in the application of the wide bandgap semiconductor materials, diamond and SiC, for power electronics. Several of the properties of these materials, including high operating temperature, high thermal conductivity, high saturation velocities for charge carriers, and high breakdown voltages, suggest that these materials have potential to far out perform conventional semiconductors in electronic applications. Several figures-of-merit, which indicate the relative potential of elemental and compound semiconductor for high power applications, have shown that α-6H-SiC has significant advantages over Si, GaAs, and GaP [1]. While these figures-of-merit are convenient in providing an initial indication of the material performance, only the large signal simulation of a specific electronic device with experimentally measured material parameters will provide a reliable indication of the advantages of these materials. The use of such a device model makes it possible to adjust design parameters so that the material characteristics that improve performance are maximized, while any detrimental material effects are removed or limited.

Presented here are the results of an investigation into the simulated performance of 6H-SiC double -drift IMPATT diodes. A large-signal device physics model of an IMPATT diode, based upon drift/diffusion carrier transport (i.e., Boltzmann transport) and electric field

* The following is a preprint of a paper recently completed and submitted for publication.

dependent impact ionization, is employed to study SiC at the four frequencies of 35, 44, 60, and 94 GHz.

The large-signal model used considers only carrier transport and carrier generation in evaluating the performance of a semiconductor material. Such constraints as the thermal conductivity and load impedance matching are used to determine the optimum current density and device area for a particular frequency. These constraints allow for the comparison of SiC diodes to the actual performance of conventional IMPATTs.

B. Material Parameters

The RF performance of 6H-SiC IMPATT diodes is determined by both the structural design (i.e., doping levels and layer thickness) and the electronic transport properties of the material. Electronic material parameters of interest are electron and hole transport characteristics as described by the mobile charge carrier velocity-field and diffusion-field characteristics. A list of the cogent parameters is given in Table I.

Table I. Material Parameters for 6H-SiC Used in the IMPATT Simulations.

Parameter	Value
Hole Mobility (μ_p)	50 cm^2/V-s
Hole Saturation Velocity (v_{psat})	5.4×10^6 cm/s
Hole Diff. Coef. (D_p)	0.55 cm^2/s
Electron Mobility (μ_n)	250 cm^2/V-s
Electron Saturation Velocity (v_{nsat})	2.0×10^7 cm/s
Electron Diff. Coef. (D_n)	9.88 cm^2/s
Ionization Constants	
(α_p)	$4.65x\times10^6$ cm^{-1}
(α_n)	4.65×10^4 cm^{-1}
($\beta_{n,p}$)	1.2×10^7 V/cm
Dielectric Constant (ε_r)	9.7
Thermal Conductivity (κ_T)	5 W/cm-°C

Experimental velocity-field characteristics have been reported for 6H-SiC [2,3]. The velocity-field characteristics for both electrons and holes for several semiconductors are compared in Figures 1 and 2. The saturation velocity for electrons in 6H-SiC is 2×10^7 cm/s at room temperature for nitrogen doped SiC (with $n=10^{17}$ cm^{-3}). From Figure 1, it is observed that the saturation velocity for electrons in a 6H-SiC exceeds that of Si, InP and GaAs and

suggests that this wide bandgap material would be superior as a high frequency semiconductor. The electron low field mobility for an impurity concentration of 10^{17} cm^{-3} is 250 $cm^2/v\text{-}s$. The low field mobility for holes is between 40 and 60 $cm^2/v\text{-}s$ for a carrier concentration of 5×10^{15} cm^{-3}, but hole saturation velocity is still undetermined.

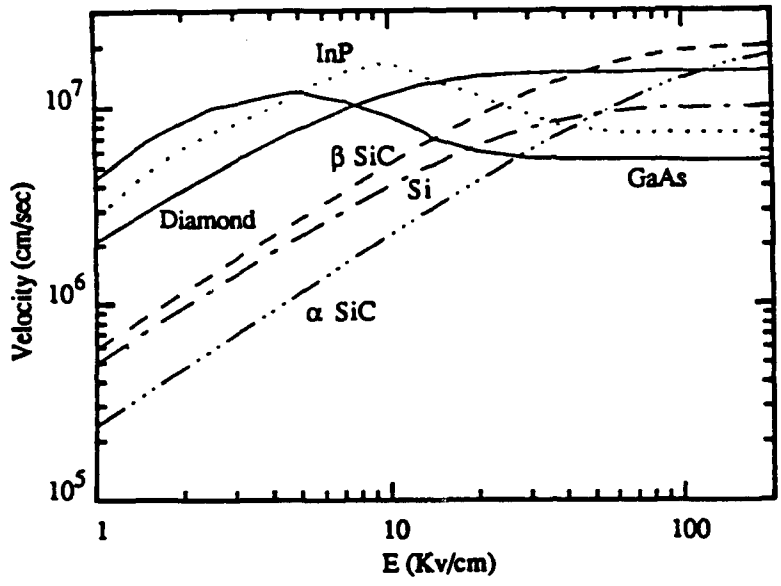

Figure 1. Electron velocity vs. electric field for several semiconductors at $N_D = 10^{17}$ cm^{-3}.

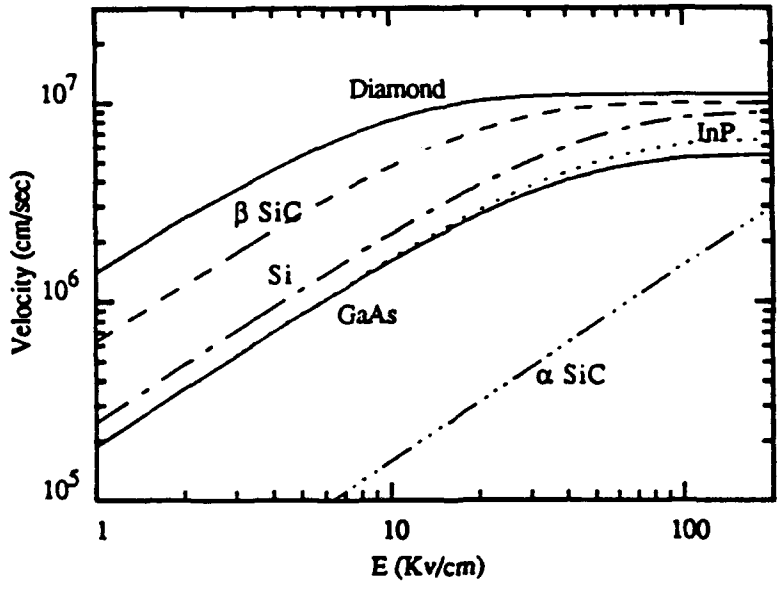

Figure 2. Hole velocity vs. electric field for several semiconductors at $N_D = 10^{17}$ cm^{-3}.

The saturation velocity for holes in SiC is estimated to be about 5.4×10^6 cm/s. This value of saturation velocity allows the holes and electrons to saturate at the same electric field (approx. 2-300 kV/cm). While it might be reasonable to assume a saturation velocity for holes

in SiC equal to that of electrons, the electric field necessary for saturation to occur would be 3 to 4 times greater. In an IMPATT diode, where carriers move across the active region at the saturation velocity, the minimum electric field could exceed 1 MV/cm. An electric field of this magnitude would produce significant avalanche throughout the device.

Because of the lack of information regarding the diffusion coefficient, the Einstein relationship is used to calculate the diffusion coefficients from the mobility measurements. A constant value for the diffusion coefficients is assumed.

While many investigators have reported avalanche breakdown in 6H-SiC [4-7], two have considered the effect of the direction of the electric field relative to the *c* axis of the hexagonal crystal [8,9]. Dmitriev, et. al., find 6H-SiC to be strongly anisotropic with respect to avalanche breakdown. Epitaxial 6H-SiC is typically grown in the *c* direction and conventional IMPATT diode fabrication would produce devices with the electric field also in the *c* direction. Dmitriev finds that the process of impact ionization is decisively influenced by superstructure splitting in the conduction band and that holes dominate the carrier generation. The avalanche generation by electrons is considered insignificant. Anikin, et. al., also find the avalanche breakdown to be anisotropic and dominated by hole generation, but believe that the avalanche mechanism involves deep level states corresponding to residual impurities and not the conduction band superstructure. While only the ionization rates and not the avalanche mechanism are needed to perform initial device simulations, future simulations might need to consider the effects of temperature and current density on the avalanche generation rates. The ionization rates when the field is parallel to the *c* axis are as follows:

$$\beta_p = 4.65\times10^6 exp(-1.2\times10^7/E)$$

and

$$\alpha_n = \beta_p/100$$

where β_p and α_n are the ionization rates for holes and electrons, respectively, and are given per centimeter. Avalanche rates have not been reported for electrons, but are considered insignificant. In these simulations, electron avalanche rates were assumed to be about 1 % of the value found for holes.

C. SiC IMPATT Performance

The dopant levels and thicknesses for the layers of the double-drift, uniformly doped 6H-SiC IMPATT diodes were optimized to provide the maximum RF output power. These SiC profiles differ from the design found for the other semiconductors, due to the requirements that holes initiate the avalanche current and to the poor transport properties of SiC holes, as indicated in Table II.

Table II. Optimized Profiles for SiC Double Drift IMPATT Diodes.

Freq (GHz)	p-region Doping (10^{17} cm^{-3})	P-Width (μm)	n-region Doping (10^{17} cm^{-3})	n-Width (μm)
35	1.50	1.00	0.63	2.30
44	1.80	0.90	1.00	1.70
60	2.20	0.75	1.15	1.40
94	2.50	0.60	1.50	1.10

For 6H-SiC, with it's higher thermal conductivity and breakdown voltage, the use of the same current densities that are acceptable for Si or GaAs would be misleading in the comparison. In order to include these additional factors in the evaluation of SiC IMPATTs, an area-current density *(A-J)* analysis procedure devised by Blakey and Linton is employed [10]. This technique establishes the limits of allowed combinations of device area and dc current density. The allowed combinations are limited by several mechanisms. These mechanisms include thermal limitations, space-charge induced field perturbations, the minimum diode impedance, and the avalanche resonance limit for current density, as described by Gilden and Hines [11]. Each of these limitations gives rise to a boundary in the *A-J* plane between allowed and unallowed combinations of device area and current density. The location of each of these boundary lines is a function of the material, the diode structure, and the frequency.

An example of the *A-J* analysis for the 44 GHz SiC IMPATT is presented in Figure 3. For this IMPATT diode and the other SiC diodes investigated, RF power was limited by the thermal resistance and the high breakdown voltages.

For CW operation this analysis, in conjunction with the large signal model, predicts maximum RF output power for SiC IMPATTs to be about 2.1 W at 35 GHz, 3.26 W at 44 GHz, 3.92 W at 60 GHz, and 1 W at 94 GHz, as indicated in Table III.

In α-SiC, velocity saturation occurs when the electric field approaches 300 kV/cm. For Si, GaAs, InP and Diamond, velocity saturation requires an electric field of no more than 100 kV/cm, as indicated in Figs. 1 and 2. The higher electric field increases the portion of the applied voltage that cannot be modulated, and decreases the dc to RF conversion efficiency of the diode.

Figure 4 shows a terminal RF voltage waveform of 80 v, and the current waveforms for a 44 GHz SiC IMPATT with RF voltages of 80, 110 and 130 v. The RF voltage of 80 volts is about 20% of the dc voltage that is applied to the SiC diode, which is biased with a dc voltage of 440 v. For materials such as diamond and GaAs, the optimum RF voltage that can be supported by the diode is greater than 50% of the dc voltage. When the RF voltage is increased

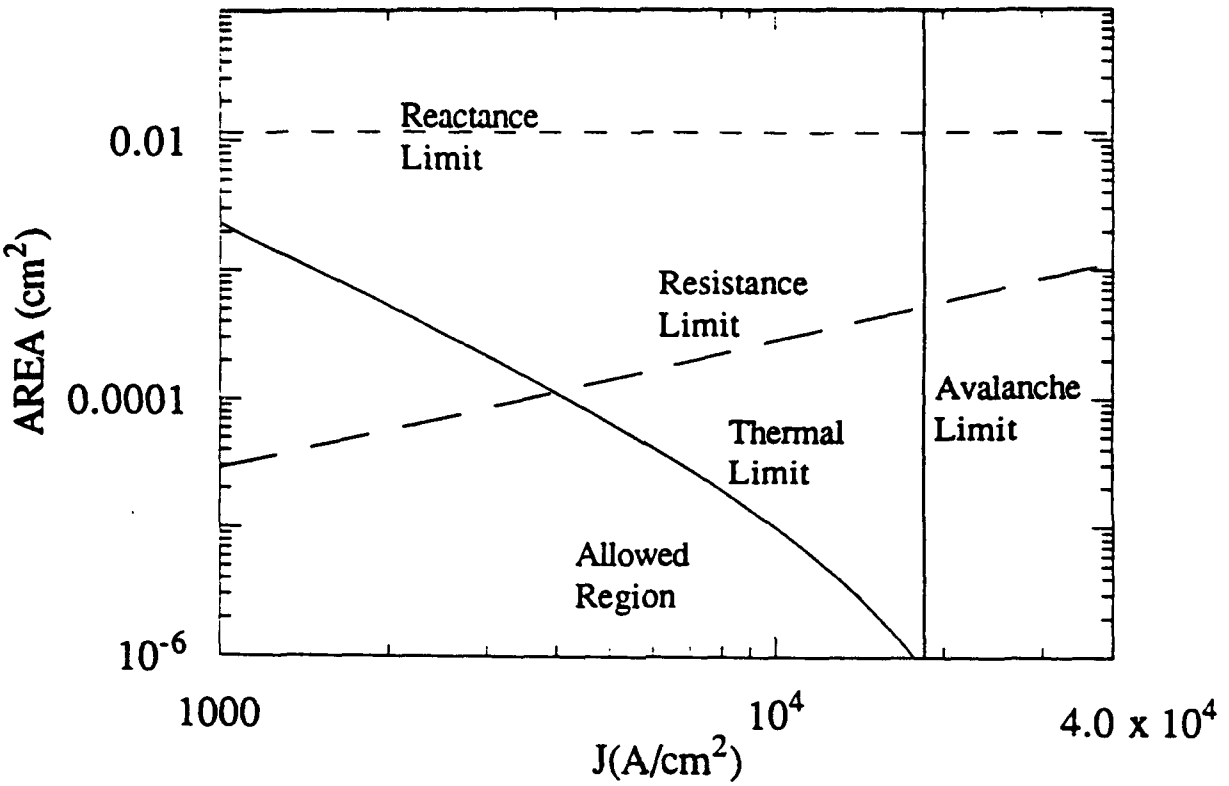

Figure 3. A-J plane analysis: a technique for IMPATT diode optimization. The analysis for a 44 GHz diode is shown.

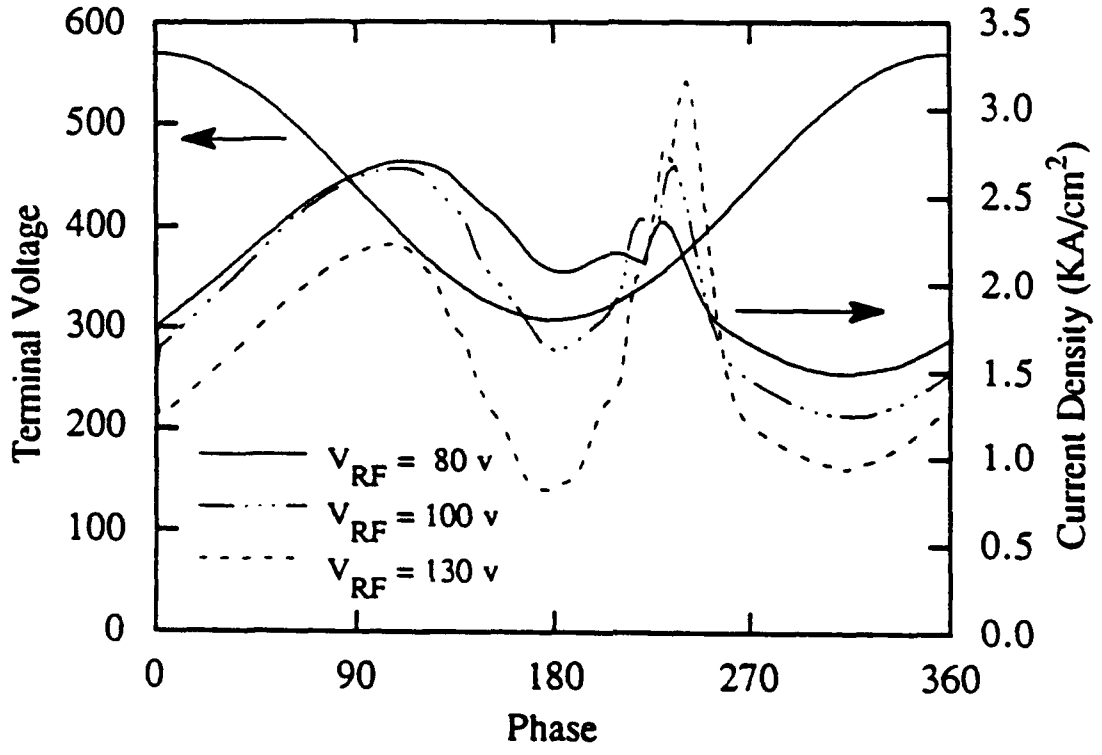

Figure 4. The terminal current vs. phase for a 44 GHz SiC IMPATT for RF voltages of 80, 100, and 1130 volts. The terminal voltage waveform for 80 volts is included.

for the SiC device, the limitations due to the low mobility of the holes become apparent. As the magnitude of the RF voltage is increased, there is a drop in the terminal current near 180 degrees. This occurs because the terminal voltage has dropped to its minimum at 180 degrees and the electric field has fallen below the level necessary to maintain the charge carriers at their saturated velocity. As the terminal voltage increases, the electric field rises and the terminal current rises again. It is the low field mobility of holes that limits the magnitude of the RF voltage that can be supported by SiC IMPATTs. This effect has also been observed in the simulation of diamond and GaAs IMPATTs under large RF voltage conditions, but the effect is not as severe as for SiC.

Table III contains the CW performance and, in some cases, the current density and area were adjusted to investigate the change in RF output power and efficiency. Higher current density increases the efficiency of the SiC diodes, but the thermal limitations decrease the diode area and usually decrease the RF output power. The performance of SiC IMPATTs is compared with other materials in Figure 5. While the RF output power for SiC devices is similar to Si and GaAs IMPATTs, the dc to RF conversion efficiency for SiC diodes is much less.

Table III. SiC Diode CW RF Performance Chacteristics.

Freq (GHz)	Area (cm^{-2})	J (kA/cm^2)	I (mA)	Vdc (V)	PRF (W)	η (%)
35	7.0×10^{-5}	4.0	280	512.4	2.10	1.7
35	2.3×10^{-5}	6.0	138	517.2	0.92	1.6
44	1.1×10^{-4}	4.0	440	436.9	3.26	1.8
44	2.0×10^{-5}	8.0	160	425.6	0.25	2.1
44	2.0×10^{-6}	15.0	30	426.2	0.36	3.2
60	3.3×10^{-5}	3.0	100	355.9	0.21	0.6
60	5.6×10^{-5}	5.0	280	352.1	.84	1.88
60	2.9×10^{-5}	8.5	247	372.7	3.92	4.28
94	3.8×10^{-5}	10.5	400	243.1	1.03	1.1
94	2.1×10^{-6}	28.6	60	236.3	0.42	3.0

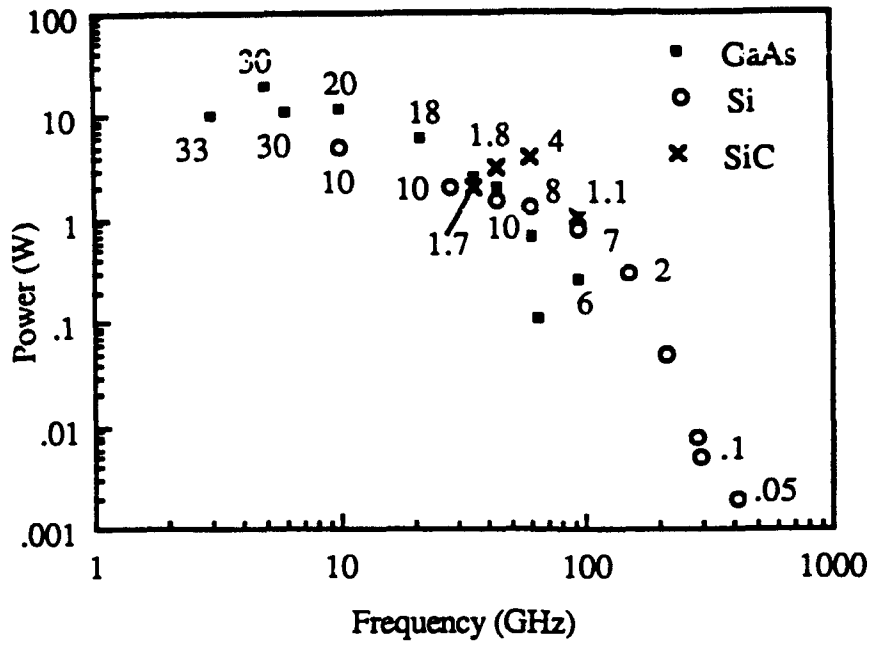

Figure 5. The output power for GaAs, Si and SiC IMPATT diodes. Numbers represent power conversion efficiency (%).

The saturation velocity of holes was assumed to be 5.4×10^6 cm/s. Although there is uncertainty in the actual value for the hole saturation velocity due to a lack of measurements, and the actual value could possibly be higher than the value assumed here. A higher saturation velocity would require a longer p-region to maintain a constant time delay as the holes traversed the drift region. Also, due to the low mobility of holes, the minimum electric field necessary to maintain velocity saturation would increase. The increases in device length and minimum electric field would increase the applied voltage, and increase the dc power dissipation, thereby enhancing thermal degradation. The thermal limitation could be eleviated by pulse bias operation.

Although the RF performance of double drift diodes in SiC is limited by the low mobility of holes and the need for holes to generate the avalanche current, this investigation indicates that single drift IMPATT diodes should perform much better than similar diodes fabricated from conventional semiconductors. In a single drift p^+n SiC diode, holes initiate the avalanche and constitute the avalanche current that flows across the junction. The low mobility of SiC holes suggests that the hole diffusion coefficient would also be low and the diffused holes would remain close to the junction. This would limit the width of the avalanche region for the diode and decrease the avalanche voltage. The additional holes that are generated in the n-region of the SiC would be swept towards the junction and collected. These holes would move toward the junction, where the electric field strength increases, and the probability that these holes would cause additional ionization increases.

The thermal limitation of SiC diodes is reduced in single drift structures due to the lower breakdown voltages. Single drift diodes also reduce the distance between the heat producing junction and the heat sink and reduce the thermal resistance.

The dc solution for a 60 GHz SiC device as shown in Figure 6 indicates how the hole transport properties and avalanche generation control the structure of these IMPATTs. In this structure, the avalanche current is generated in the p-region of the device where there is a sufficient number of holes to initiate the avalanche current.

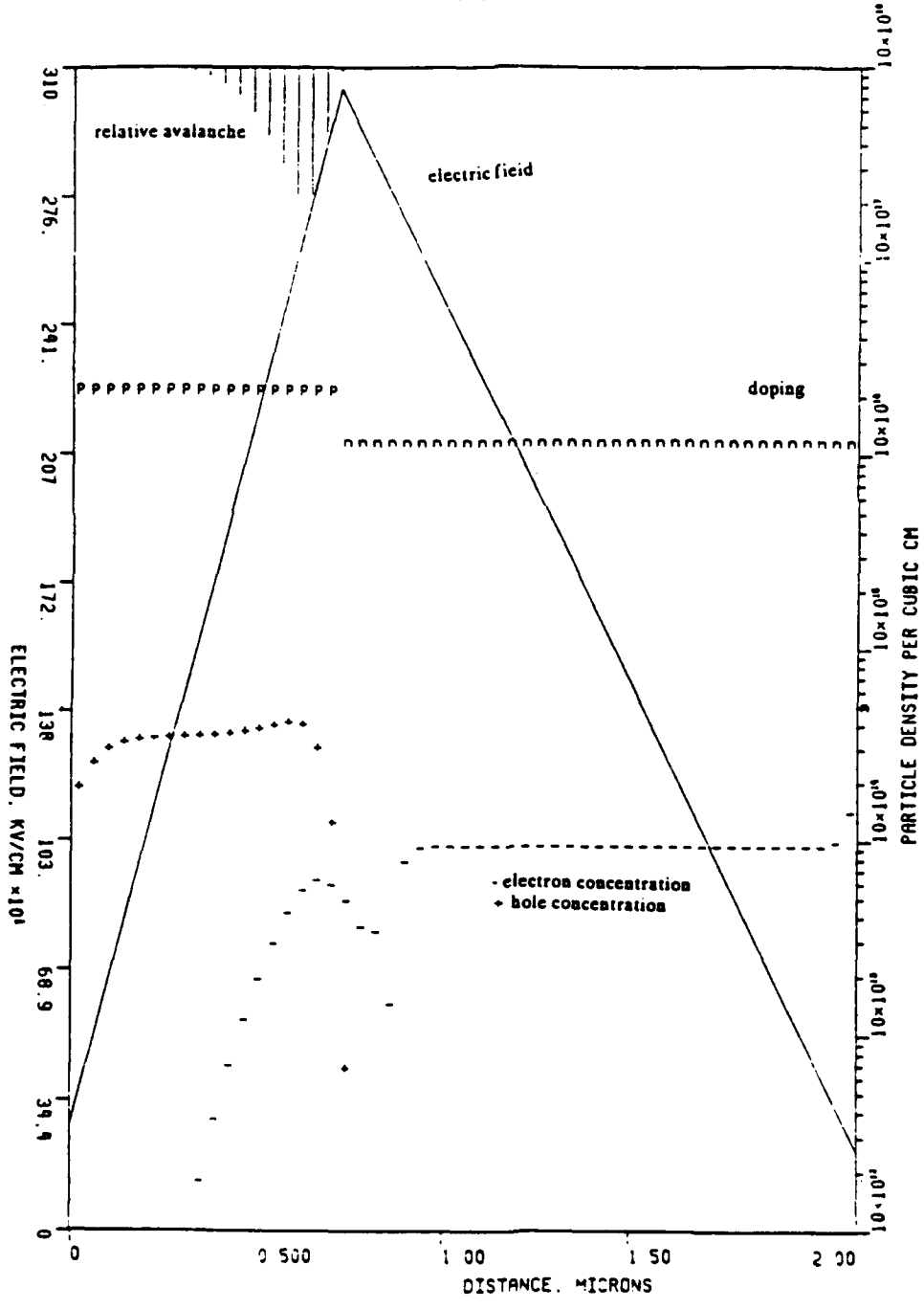

Figure 6. DC solution for the 60 GHz SiC IMPATT.

D. Conclusions

The RF performance of 6H-SiC IMPATT diodes has been investigated by means of a theoretical, physics based device model. It is found that the combination of high breakdown voltage and thermal considerations limit the practical current density at which the diodes can be operated. The problem is more severe for double-drift diode structures. Additionally, it is found that the low field mobility of holes prevent double drift SiC IMPATTs from supporting large RF voltages, thereby reducing the dc to RF conversion efficiency possible. The RF power output of SiC IMPATTs is similar to that possible from comparable devices fabricated from Si, but the conversion efficiency is significantly reduced. Possible improvements may be obtainable from single-drift, n-type devices. Such a device would have lower breakdown voltage and improved thermal resistance. The device would not rely on the transit time delay of holes and the degrading effects of the low magnitude hole mobility on conversion efficiency would be reduced.

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V. Fabrication and Characterization of SiC Devices for Microwave Applications

A. Overview

The importance of high field operation for SiC microwave performance is two-fold. The first is to obtain the high power levels that are desired at high frequency without having to make an inordinately large device. The second reason is to take advantage of the high saturated electron drift velocity (v_{sat}) of SiC (2.5×10^7 cm/sec) observed at fields above about 1.5×10^5 V/cm, as shown in Figure 1. For a MESFET operated with a source-to-drain field greater than this value, the transfer characteristics will be dominated more by v_{sat} than mobility, the latter which is quite low in SiC when compared with Si or GaAs. For an IMPATT diode, the high field capability of SiC obviously allows much more power per unit area to be delivered because it would be avalanching at much higher voltages than equivalent Si or GaAs diodes, and the high v_{sat} allows higher frequency operation. Thus, if a high frequency IMPATT diode is to be fabricated in SiC, then reliable avalanche characteristics must first be proven. Once the best configuration for avalanche operation is defined, then an IMPATT diode can be fabricated. This initial development for both high frequency MESFETs and IMPATT diodes has been achieved and is discussed below.

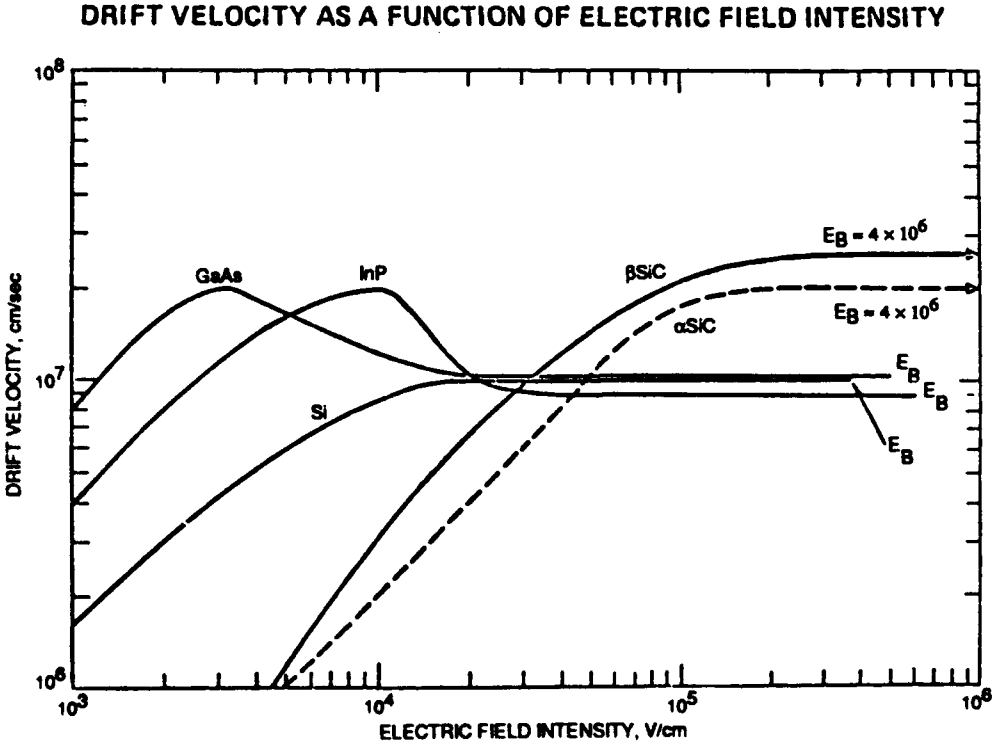


Figure 1. Electron velocity vs. electric field for several semiconductors.

B. Experimental Procedure

Substrate Preparation. The substrates used for this study were sliced from 6H-SiC crystals grown for this project. The crystals were lightly nitrogen doped n-type. The crystals were then sliced, lapped and polished into wafers suitable for epitaxial growth.

MESFET Design and Fabrication. Schottky contact samples were first characterized in order to determine the effectiveness of Pt based contacts on 6H-SiC and to see the effect of carrier concentration on these contacts. The contacts were fabricated by patterning a layer of photoresist such as to leave "doughnuts" of photoresist on n-type epilayers. The Schottky metal, Pt, was then deposited over the entire top surface. The samples were then placed in acetone which dissolved the underlying photoresist and allowed the overlying metal to "lift off" of the doughnuts. This resulted in a series of 100 μm diameter Pt dots, which act as the Schottky contacts, separated from a field of the same metal, which acts as the ohmic contact by virtue of its much larger area.

An interdigitated structure, shown in Figure 2 was used for the initial MESFET design, in order to confirm the high voltage, high power capabilities using the Pt Schottky contact on 6H-SiC. The source consisted of three "fingers" of ohmic contacts on the left, and the smaller area drain consisted of the two fingers of ohmic contacts on the right. Weaving in between these two contacts was the gate or Schottky contact. Isolation trenches were etched in the n-type top conducting layer in order to prevent leakage current around the gate contact between the source and drain. While the gate width was 1 mm for all devices, the gate length and source-to-drain distance was varied in order to determine their effect on transconductance and to be able to extrapolate what the values would be for microwave devices with much smaller dimensions. The different gate lengths were 10 μm, 13 μm, 18 μm and 24 μm, with the source-to-drain distance being 30 μm, 33 μm, 38 μm and 44 μm, respectively.

In cross-section, the device consisted of a 2 μm thick p-type expitaxial layer of 6H-SiC having a carrier concentration in the range of 1×10^{17} cm^{-3} grown on a 6H-SiC substrate. This p-type layer acted as the buried layer to confine the current to a thin n-type active region which was subsequently grown. This top n-type epitaxial layer can have a carrier concentration in the range of 3×10^{16} cm^{-3} to 3×10^{17} cm^3 and a thickness of 0.2 to 1.0 μm depending on the desired performance of the device.

Using conventional photolithography techniques, a sputtered aluminum film was patterned onto the SiC surface, which acted as a mask with which to open windows for the reactive ion etching of the isolation trenches. The trenches were etched deep enough to penetrate through the top n-type layer into the buried p-type layer. The Al was then stripped, and the sample was oxidized to grow a thin passivating layer of SiO_2. Windows for the source and drain contacts were then opened in the SiO_2 and the ohmic contacts were deposited and patterned using the "lift-off" technique. After these ohmic contacts were

annealed, the gate Schottky contact was deposited in similar fashion. Unless heat treatment of the gate contact was desired, the device was then ready for measurement.

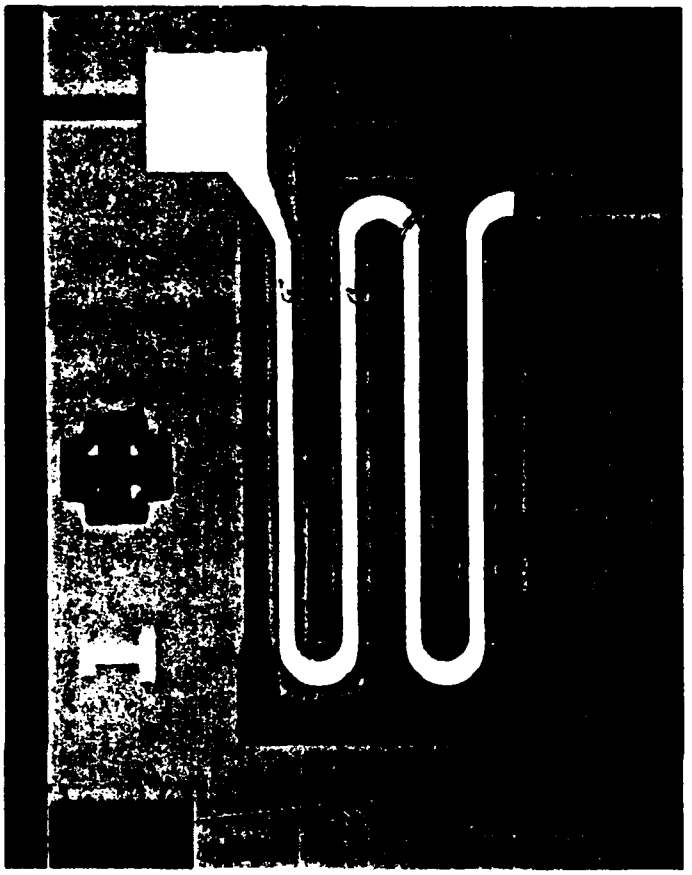


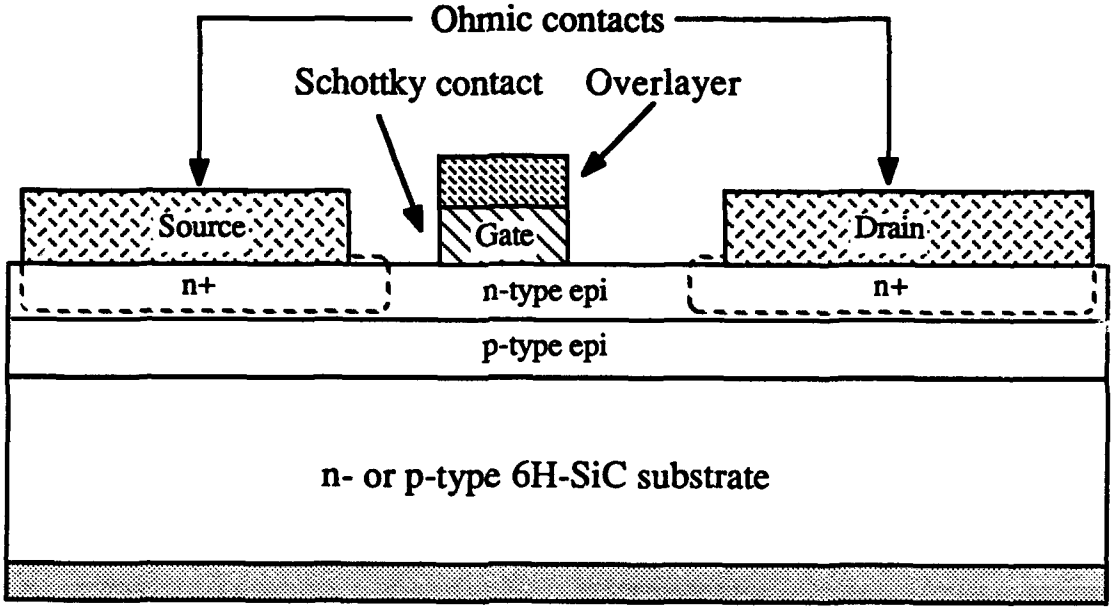
Figure 2: Interdigitated structure of a SiC MESFET. The source contact pad is at the lower left, the drain contact at the lower right, and the gate contact pad is at the upper right. This device has a gate length and width of 10 μm and 1000 μm, respectively.

The initial design of a high power-high frequency SiC MESFET is shown in Figure 3a,b. It consisted consisted of a 2 μm thick p-type expitaxial layer of 6H-SiC having a carrier concentration in the range of 5×10^{15}-4×10^{16} cm^{-3} grown on an n-type 6H-SiC substrate (Figure 3a). This p-type layer acted as the buried layer to confine the current to a thin n-type active region which was subsequently grown. This top n-type epitaxial layer had carrier concentrations in the range of 7×10^{16} cm^{-3} to 3×10^{17} cm^3 and a thickness of 0.2 to 0.48 μm depending on the doping and desired pinch-off voltage of the device.

Preliminary experiments with the above MESFETs showed that a large increase in F_{max} resulted from using a 200 nm thick overlayer of Al on top of the gate contact. The best values of F_t and F_{max} that were reported using this overlayer were 1.6 GHz and 770 MHz, respectively. At 500 MHz, the device had a power gain of 4.6 dB and a current gain

of 8.5 dB. However, further improvements in gate resistance should result in even higher frequency operation.

(a)



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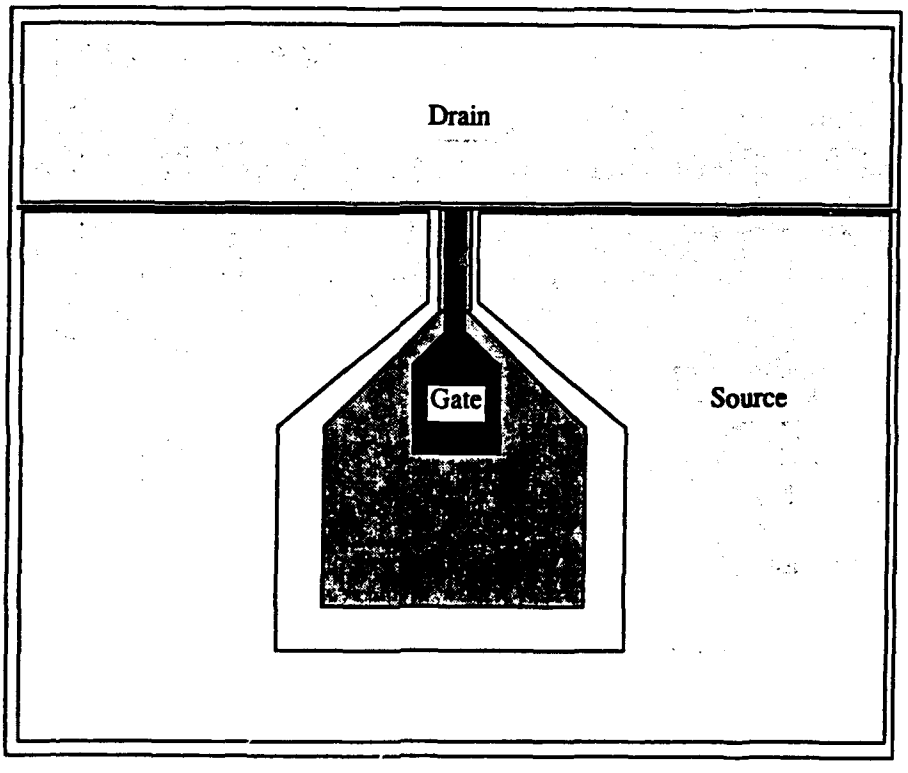

Figure 3. (a) Cross-sectional view 6H-SiC MESFET design utilizing ion implanted n^+ source and drain wells, and a buried p-type isolation layer; (b) Initial design of high power, high frequency SiC MESFET. Gate lengths vary from 4 μm to 0.8 μm, and source-to-drain distances vary from 7 μm to 2 μm. The gate width is 1 mm.

The device also had large area source and drain contacts in order to reduce the contact resistance, and the source-to-drain distances range from 7 μm down to 2 μm. The gate contact lengths range from 3 μm down to 0.8 μm. The gate width is 1 mm for all of the devices. The entire device is isolated on a mesa. Using conventional photolithography techniques, a sputtered aluminum film was patterned onto the SiC surface, which acted as a mask for the reactive ion etching of the isolation mesa. The material around the mesa was etched deep enough to penetrate through the top n-type layer into the buried p-type layer. The Al was then stripped, and polysilicon was deposited and patterned, opening windows for the source and drain pattern. The samples were then ion implanted with N^+ to form n^+ source and drain wells, using the polysilicon as the implant mask. The implants were subsequently annealed and the samples were oxidized to grow a thin passivating layer of SiO_2. In order to reduce gate capacitance, 300 nm thick layer of Si_3N_4 was then deposited over the oxide and patterned to form the center gate contact isolation pad. Windows for the source and drain contacts were then opened via reactive ion etching the nitride and then etching the SiO_2. The ohmic contacts were deposited and patterned using the "lift-off" technique. After these ohmic contacts were annealed, the fine line gate Schottky contact was deposited in similar fashion. The patterned gate consisted of only the gate "stripe" with a small 20 μm x 5 μm tab coming off of it, making the actual area of the Schottky contact very small. Contact was then made to the gate by patterning a metal pad on top of the nitride with a strip that drops over the nitride step and overlaps the gate tab. This step reduced the gate capacitance to about 4-6 pF.

In order to further improve both the device design and the fabrication procedures for 6H-SiC MESFETs, a new mask set was designed. This new design, shown in Figure 4, was still a 1 mm gate width device consisting of two 500 μm long gate fingers, but it used a much smaller source and drain ohmic contact areas that made the overall device size 27% smaller. The smaller contact area was allowed because of the n^+ source and drain to be used, as opposed to the previous design. Shorter gate lengths were used on this mask, varying from 0.6 μm to 1.0 μm. The gate - drain spacing was increased from 1 μm to 1.6 μm to allow higher drain voltages to be attained. The source - gate spacing was 1.1 μm (accounting for gate line spread) for all of the devices except the smallest gate length, which had a 0.5 μm spacing. To further reduce the gate capacitance, the gate contact pad area was reduced to the minimum value (100 μm diameter) that still allowed reliable wire bonding. Finally, source and drain metal overlayers were made to n^+ source and drain wells that were formed via high temperature N^+ implantation. Finally, source and drain metal overlayers were used to facilitate better contacting for probing as well as wire bonding.

The fabrication of these devices was as follows. The entire device was first isolated on a mesa. Using conventional photolithography techniques, a sputtered aluminum film was

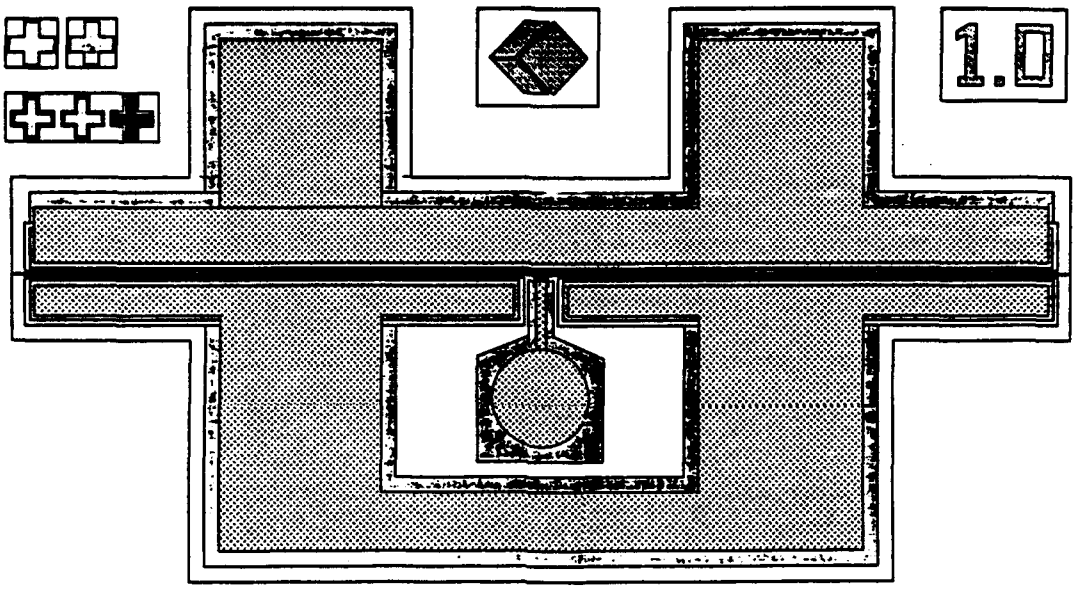

Figure 4: Design for high power, high frequency SiC MESFET. Gate lengths vary from 1.0 μm to 0.6 μm, and source-to-drain distances vary from 3.5 μm to 2.9 μm. The gate width is 1 mm.

patterned onto the SiC surface, which acted as a mask for the reactive ion etching of the isolation mesa. The material around the mesa was etched sufficiently deeply enough to penetrate through the top n-type layer into the buried p-type layer. The Al was then stripped, and polysilicon was deposited and patterned, opening windows for the source and drain pattern. The samples were then ion implanted with N^+ to form n^+ source and drain wells, using the polysilicon as the implant mask. The implants were subsequently annealed and the samples oxidized to grow a thin passivating layer of SiO_2. A 500 nm1.0 μm thick layer of SiO_2 was then deposited, using a low temperature chemical vapor deposition process, over the thin thermal oxide. This layer was patterned to form the center gate contact isolation pad and interconnect bars. Windows for the source and drain contacts were then opened in the SiO_2, and the ohmic contacts were deposited and patterned using the "lift-off" technique. After these ohmic contacts were annealed, the fine line gate Schottky contact with overlayer was patterned using an excimer laser stepper. Finally, the gate contact pad metallization was deposited and patterned on the SiO_2 isolation pad.

One of the key steps in this process scheme was the gate lithography. A process was developed for achieving fine line lithography on SiC wafers using a GCA ALS LaserStep 200 (an excimer laser stepper) at the Microelectronics Center of North Carolina on a subcontract basis. This process, which used Shipley 8843-I deep UV photoresist, resulted in much improved fine line lithography that allowed gate lengths as small as 0.6 μm to be developed. The characteristics of these fine line devices will be discussed in Section C–Results and Discussion.

Some of the devices utilized a mesa source and drain structure rather than using ion implantation. After epitaxial growth of the n-type channel layer, another n-type layer with heavy nitrogen doping was grown on top. This layer typically had a thickness of 0.2 μm and a doping of $1x10^{19}$ cm^{-3}. The source and drain were defined by reactive ion etching the n^+ layer away except where the source and drain contacts were to go, using the same mask as was used for the ion implants. The insulator layers and gate contacts were then deposited on the etched back channel layer, just as was done for the devices previously discussed.

IMPATT Diode Design and Fabrication. The initial modeling for IMPATT diodes was for operation at 60 GHz using a flat profile for the drift layer, and showed that this epilayer must have $n = 4x10^{16}$ cm^{-3} and a thickness of 2 μm. This thickness and carrier concentration are dictated by that desired frequency. Unfortunately, the carrier concentration in turn dictates that the avalanche will occur at voltages in the range of 350-400 V for SiC. This is a demanding voltage from the aspect of junction quality and passivation. While these voltages have certainly been achieved for SiC pn junction diodes, it requires special structures and passivation techniques that may not readily transfer into a desirable IMPATT fabrication scheme. Therefore, more modeling was performed so that a "high-low" structure could be used, in which the avalanche takes place at a relatively low voltage in a more heavily doped layer, and the drift takes place in a lightly doped layer. The modeling showed the most desirable doping profile for a high-low structure to be a 0.2 μm thick "high" layer with $n = 4.5x10^{17}$ cm^{-3}, and a 1.2 μm thick "low" layer with $n = 3x10^{16}$ cm^{-3}. Both the "flat" profile and the "high-low" structure were fabricated. Regardless of the breakdown structure, the same set of masks were used. Seven different diameter dots, varying from 38.1 μm to 381 μm, were designed in order to find the device area that yielded the best impedance matching.

These first IMPATT structures were based on pn junction diodes. The initial design for SiC IMPATTs used a mesa pn junction structure with a passivated sidewall. A variety of epilayer structures were grown so that the best configuration could be determined. Both p^+-n and n^+-p flat profiles were fabricated, as well as the p^+-n^+-n^- high-low structure discussed above. The epilayers were all grown on n^+ substrates for maximum conductivity, and then mesas were reactive ion etched in the SiC to a depth of 14 μm. The sidewalls were passivated via thermal oxidation, and the p-type ohmic contacts were defined and annealed on top of the mesas. The substrates were then thinned to about 60 μm thick, and ohmic contacts were deposited on the backside of these wafers, which were subsequently annealed. None of these structures showed promising avalanche characteristics, because of the amount of sub-avalanche reverse bias leakage current. Most of the devices had a leakage current of about 1 mA at a reverse bias of 30 V, which was well below the avalanche voltage.

In the "high-low" design for low voltage avalanche. Both pn junction and Schottky diode structures were made. Both structures had the same epitaxy for the breakdown layers, as is shown in Figure 5. The starting substrates were n-type that were doped with nitrogen so that n = 1-3×10^{18} cm^{-3}. The first epilayer, which serves as the drift layer, was then grown with a thickness of 1.2 μm and a carrier concentration in the range of 3×10^{15}–4×10^{16} cm^{-3}. This layer was followed by a more heavily doped avalanche layer with a thickness of 0.22 μm and carrier concentration in the range of 3×10^{15}–5×10^{17} cm^{-3}. The samples for the Schottky diode IMPATTs were then ready for processing. The pn junction IMPATT wafers had a subsequent p^+ layer grown on them that was 0.8 μm thick and had a carrier concentration of p = 3-5×10^{18} cm^{-3}.

The device fabrication for the IMPATT diodes involved first thining the wafers to 125 μm thick by diamond grinding the backside of the wafer. The diode mesas were then formed via reactive ion etching using Al as the mask material. The mesas were etched through the epilayers into the n^+ substrate. The samples were then oxidized in dry O_2 to form a passivating layer of oxide on the mesa sidewalls. Using photolithography, windows were etched in the oxide for the topside Schottky or ohmic contacts, depending on whether the wafers were Schottky or pn junction IMPATTs, respectively. The topside contacts were then formed on the front and backside of the wafer as shown in Figure 5. The one difference is that the backside via shown in Figure 5 was not fabricated because of thedifficulty in handling the very thin wafers. When the optimal device structure is determined, future devices will have these backside vias etched in them. The reason for

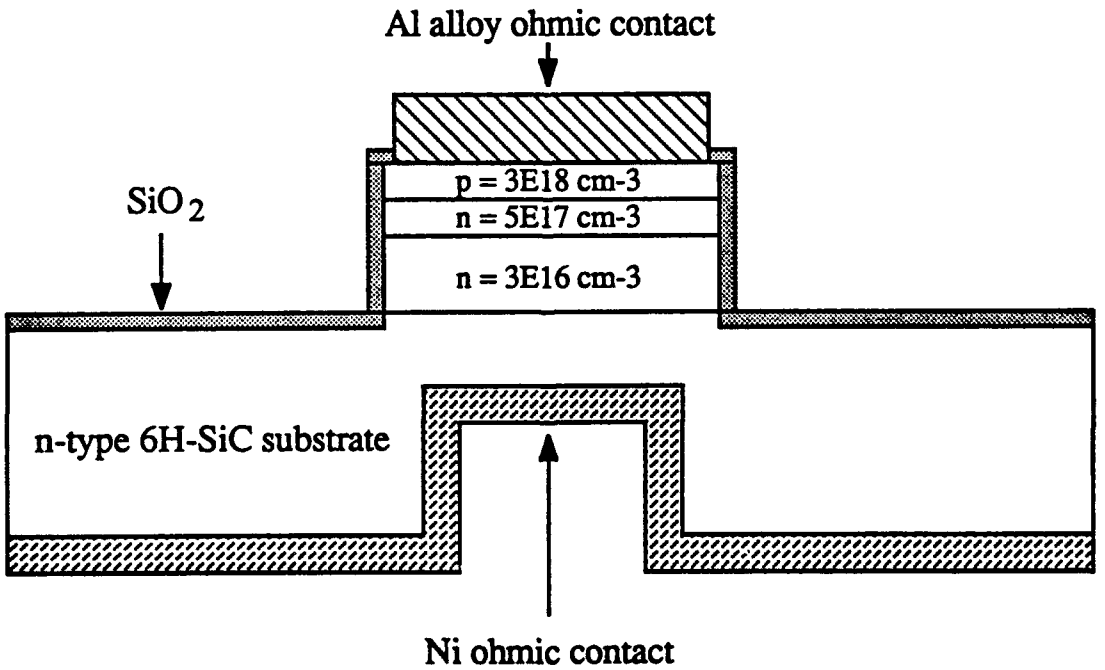

Figure 5. Cross-sectional view of p-n junction "high-low" IMPATT diode structure in 6H-SiC.

these vias is to reduce the substrate resistance, allowing higher frequency operation. Ideally, this via would be etched as deep as 100 μm, giving a 25 μm distance from the drift layer to the ohmic contact. In practice, the etch depth will probably be in the range of 25-50 μm because of wafer breakage problems. The same set of masks were used for both Schottky and pn junction IMPATTs. Seven different diameter dots, varying from 38.1 μm to 381 μm, were used in order to find the device area that yielded the best impedance matching.

C. Results and Discussion

MESFET Characterization. An I-V curve at room temperature of one of the initial SiC MESFETs having the interdigitated structure shown in Figure 2 is shown in Figure 6(a). This device had a gate length of 13 μm, a gate width of 1 mm, and a source to drain distance of 33 μm. The device shows good current saturation to $V_D = 40$ V, although there is some non-uniformity at the intermediate gate voltages. The maximum transconductance was 1.5 mS/mm and the threshold voltage is -4.4 V. The subthreshold leakage is quite low, having a value of 44 μA at $V_D = 40$ V and $V_G = -6$ V. The MESFET's I-V characteristics actually improved when heated to 100°C, as shown in Figure 6(b). The maximum transconductance increased to 1.65 mS/mm, and the current saturation was quite good to $V_D = 30$ V, with some leakage still present at higher drain voltages. The subthreshold leakage current was 52 μA at $V_D = 40$ V and $V_G = -6$ V. When heated at 200°C, the I-V characteristics were virtually identical to those shown at 100°C. The I-V characteristics at 300°C are shown in Figure 6(c). The subthreshold leakage increased to 96 μA at $V_D = 40$ V and $V_G = -6$ V, and the maximum transconductance decreased to 1.26 mS/mm, but overall these were promising characteristics. While these particular devices also operated at 400°C, they were unfortunately ruined by holding at this temperature for too long in air. However, it is assumed that if the device was hermetically sealed in a package containing an inert atmosphere, that the devices would have operated to much higher temperatures, indicating that high power MESFETs will withstand a large amount of self-heating.

Improved control over doping and crystal quality led to the fabrication of MESFETs with improved high voltage capability, as shown in Figure 7. This device had a source-to-drain distance of 44 μm and a gate length of 24 μm. Drain voltages of 100 V were achieved without breakdown or significant leakage. The current levels were also quite high compared to those shown in Figure 6, with power capability at a drain voltage of 100 V being in excess of 4 W per mm of gate width. The maximum transconductance was also higher, at 4.3 mS/mm. The subthreshold leakage current at $V_d = 100$ V and $V_g = -18$ V was 325 μA. Since high field operation is desired for a SiC high frequency MESFET,

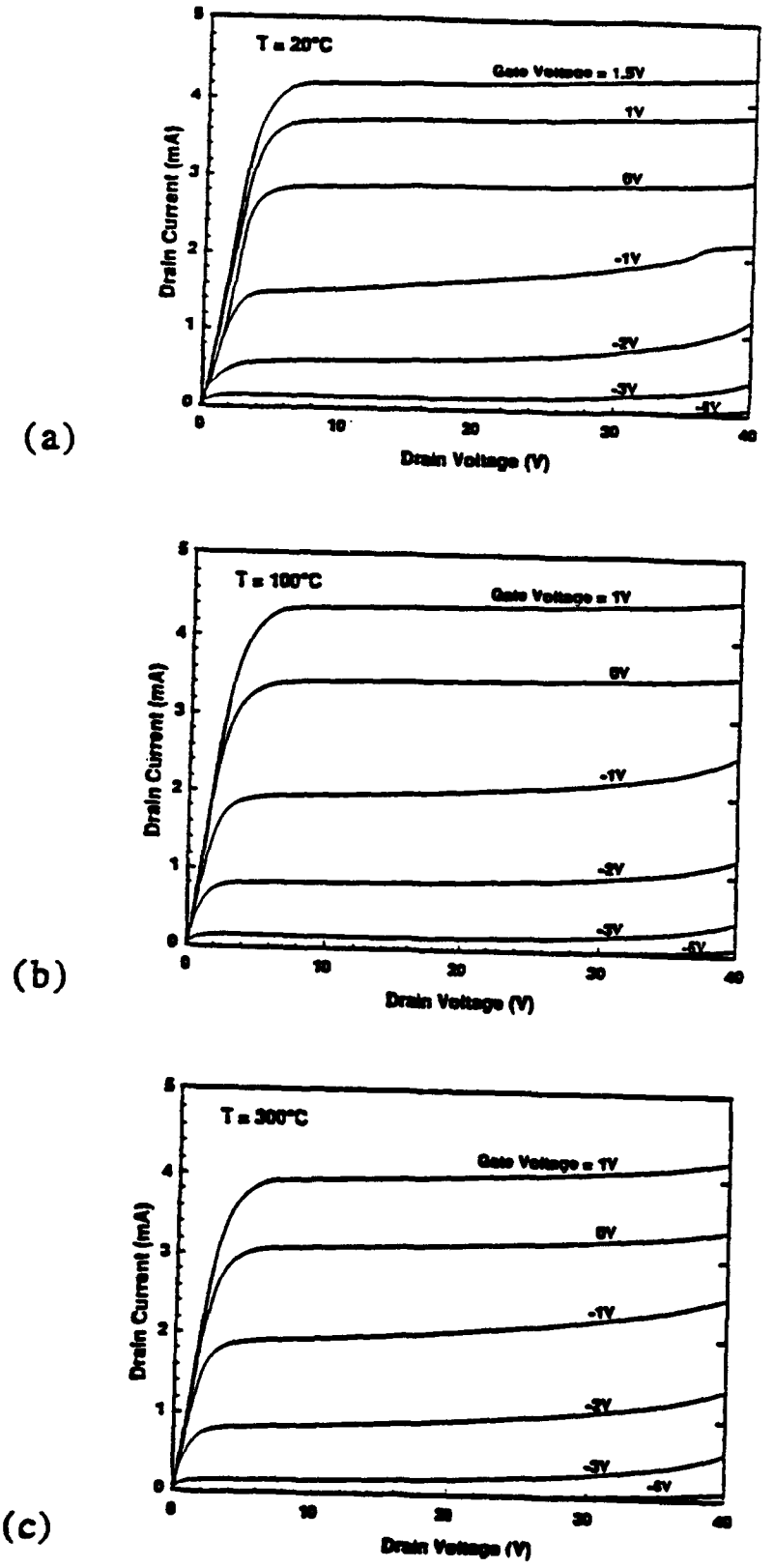

Figure 6. Drain current-voltage characteristics, after an anneal, of a SiC MESFET at (a) 20°C, (b) 100°C, and (c) 300°C.

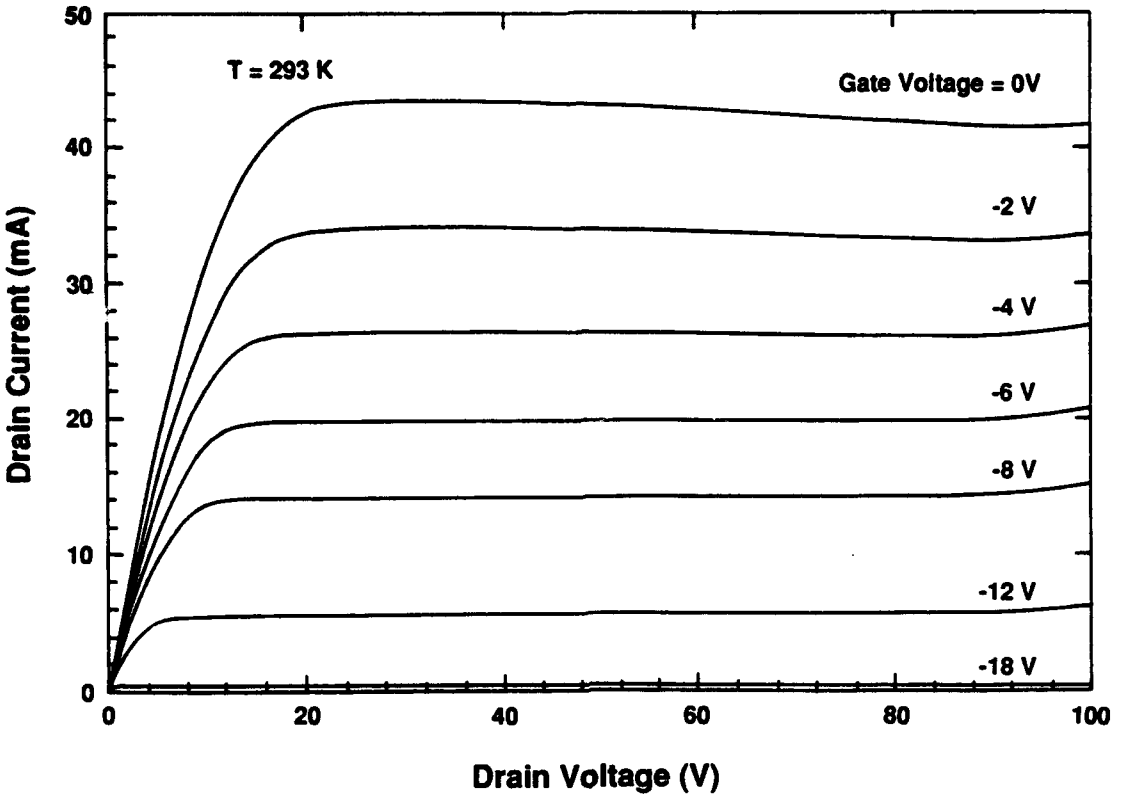

Figure 7. Drain current-voltage characteristics of a SiC MESFET demonstarting V_d = 100 V capability. Gate length and width are 24 μm and 1mm, respectively.

these results were very promising. The remaining task is to translate this high field capability of the Schottky gate into a much smaller dimension gate length and a much smaller source-to-drain distance.

High-power, high frequency devices with these smaller dimensions have been fabricated using the design illustrated in Figure 3. The n-type channels had a doping level of n = 0.8-3 x 10^{17} cm^3 and a thickness of about 200-400 nm, with buried p-layers (p = 1-4×10^{16} cm^{-3}) underneath. A typical I-V curve of one of these MESFETs is shown in Figure 8. This particular device had a source-drain distance of 4 μm and a gate length of 2 μm. The curve shows that a drain voltage of 30 V was obtained with a gate voltage of -6 V. The maximum transconductance of this device was 6.4 mS/mm and very stable current saturation was observed to V_{DS} = 30 V. This device was measured on at high frequency using an HP 8510 automatic network analyzer with a Cascade Microprober for standard S-parameter measurements. The plot in Figure 9 shows that this device has a threshold frequency (F_t) of 510 MHz, designated where the H21 parameter crosses 0 dB gain. The power gain (G_{max}) crosses 0 dB at about 380 MHz, indicating that F_{max} is at least 380 MHz.

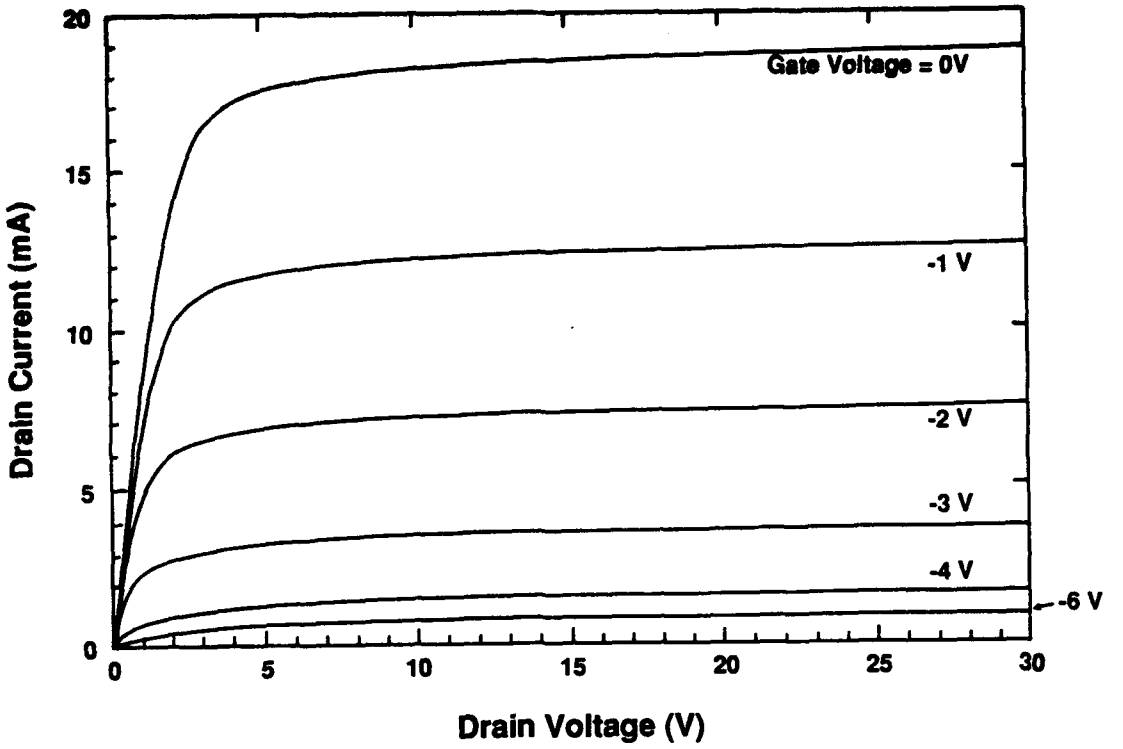

Figure 8. Drain current-voltage characteristics of a SiC MESFET using high power high frequency mask shown in Fig. 3. Gate length and width are 2 μm and 1 mm, respectively. Source-to drain distance is 4 μm. The maximum transconductance is 6.4 mS/mm.

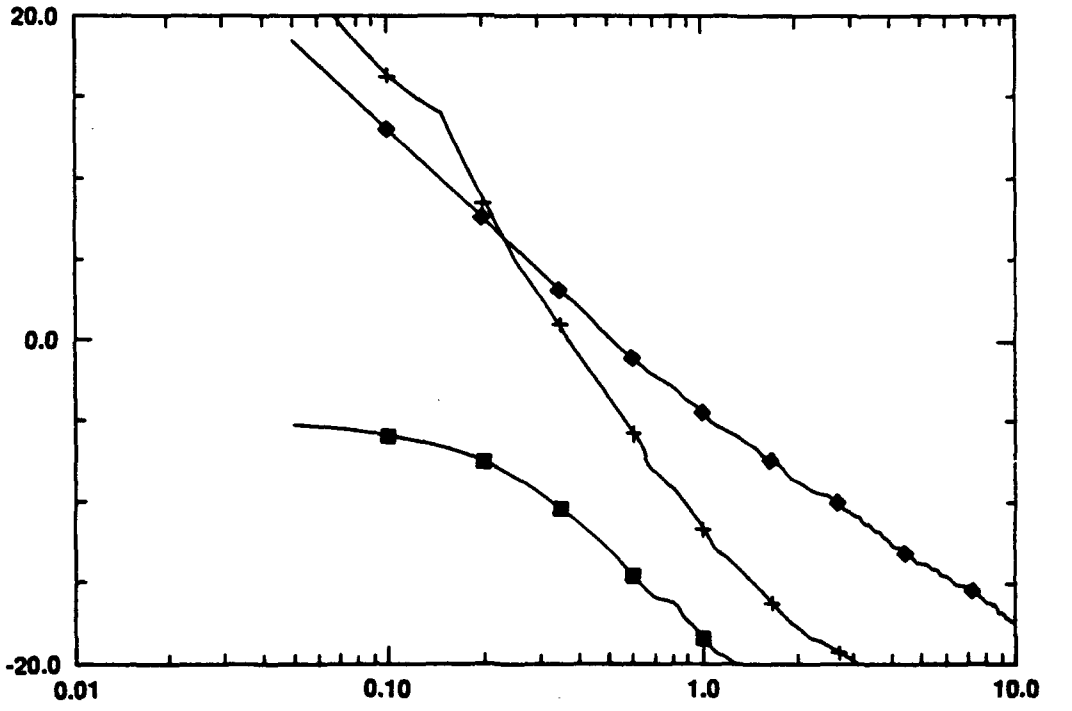

Figure 9. High frequency parameters, S21, G_{max}, and H21, as a function of frequency for the 2 μm gate length device. Measurement conditions were V_D = 30 V, I_D = 14.2 mA, V_G = -1.0 V, and I_G = 1 μA.

A gain vs. frequency plot for a shorter gate length device is shown in Figure 10. This device had a gate length of 1.7 μm and had a correspondingly higher gain. The F_t of this device was 800 MHz and the F_{max} was at least 450 MHz. At 250 MHz the device had a current gain of 10 dB. While the high frequency gain always increased with decreasing gate length, as it should, the DC transconductance seemed to be virtually independent of gate length. For instance, the highest transconductance observed to date was 22 mS/mm for a 4 μm gate length device. Figure 11 shows a MESFET with a 2 μm gate length that had a relatively high transconductance of 12.3 mS/mm but still had a relatively short gate length. Although this device had a high on-current (>200 mA), it could not be cutoff because the channel was too thick. This device had the best high frequency gain of the devices measured, as shown in Figure 12. It had an F_t of 900 MHz and a F_{max} greater than 450 MHz.

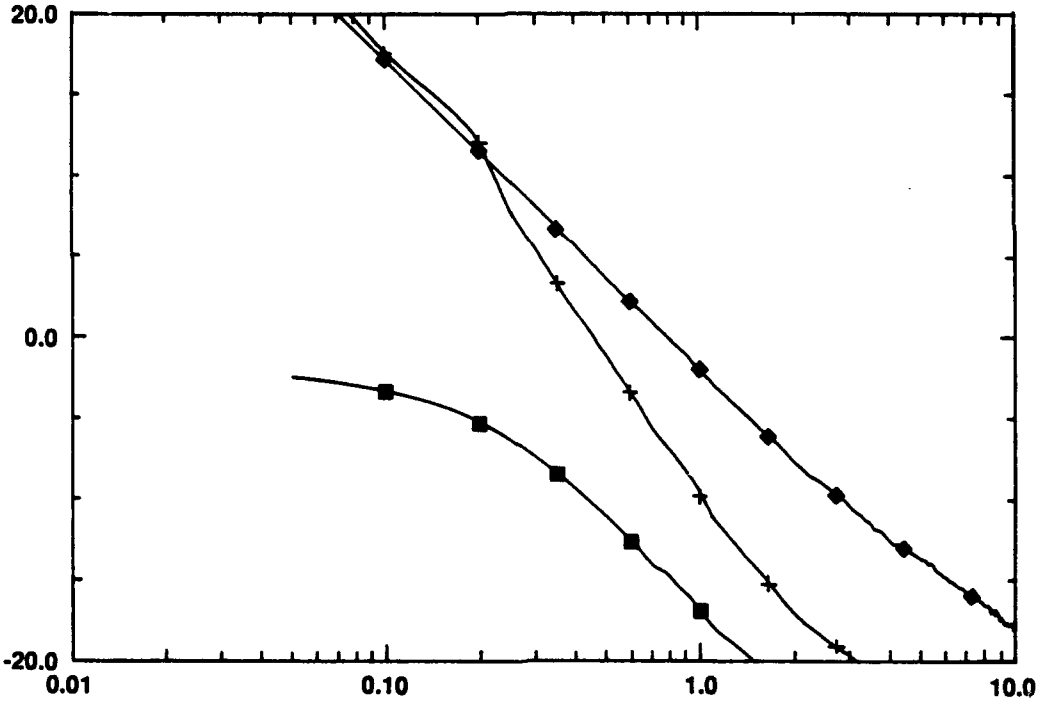

Figure 10. High frequency parameters, S21, G_{max}, and H21, as a function of frequency for a 1.7 μm gate length device. Measurement conditions were V_D = 30 V, I_D = 68.4 mA, V_G = -1.0 V, and I_G = 1.7 μA.

The observed DC transconductances were quite low when compared to the long gate length device shown in Figure 7, considering the much smaller gate lengths and source-drain distances used in the high frequency design. This indicates that the limiting parasitic resistance is not related to mobility between the source and drain, but rather to contact resistance at the source and drain. It is apparent that the source and drain resistance are so

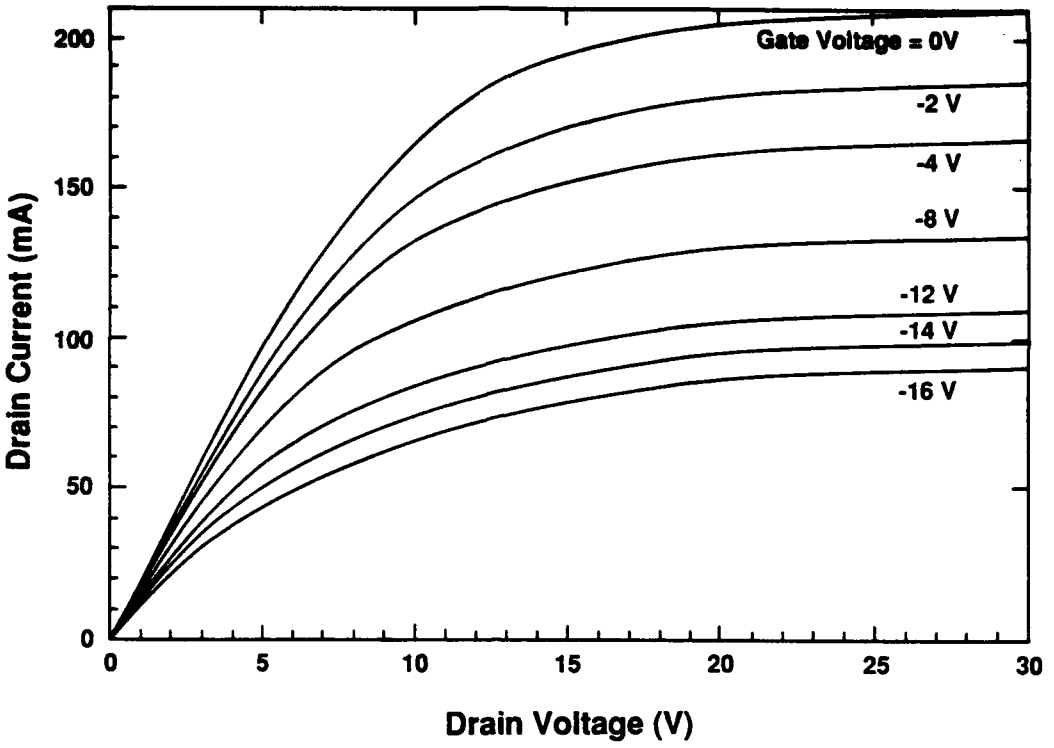

Figure 11. Drain current-voltage characteristics of a SiC MESFET. Gate length and width are 2 μm and 1 mm, respectively. Source-to drain distance is 4 μm. The maximum transconductance is 12.3 mS/mm.

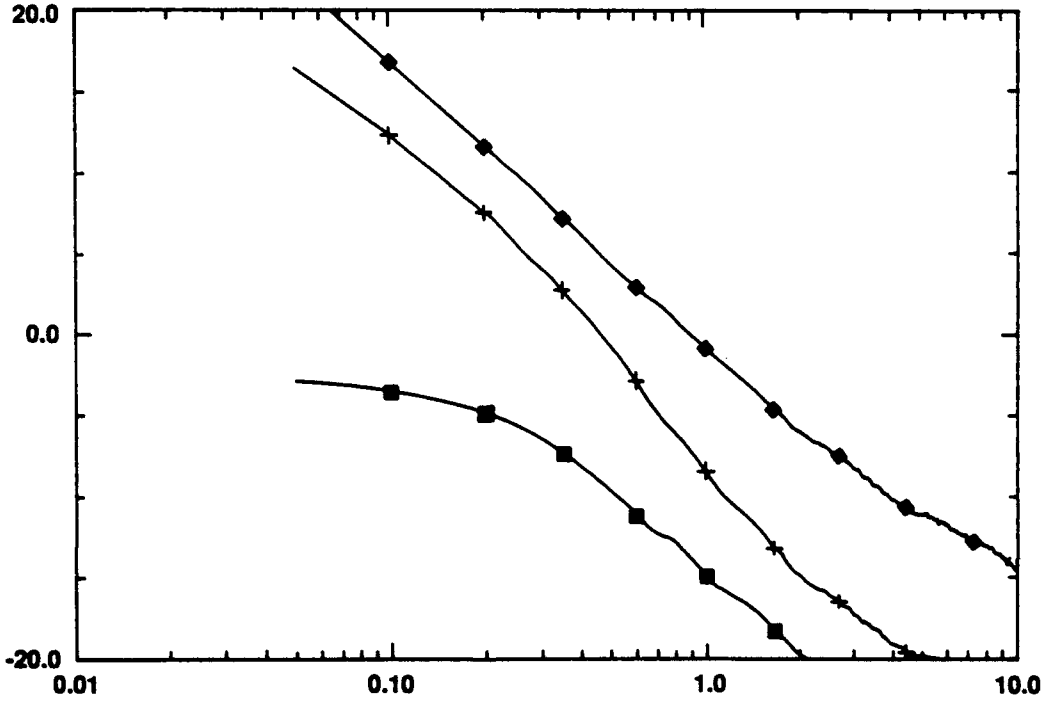

Figure 12. High frequency parameters, S21, G_{max}, and H21, as a function of frequency for the 2 μm gate length device shown in Figure 19. Measurement conditions were V_D = 30 V, I_D = 189 mA, V_G = -1.0 V, and I_G = 1 μA.

dominant that the effect of reducing the gate length and source-drain spacing on the DC transconductance is negligible. The high frequency measurements show the effect of gate length because transit-time still plays a role, however, it is proposed that the overall high frequency gain of all of the devices was severely limited by the parasitic source and drain resistances. As such, the next iteration of 6H-SiC MESFETs was studied via modeling and subsequently fabricated with n^+ source and drain wells, as is common practice even for GaAs MESFETs.

The positive benefits of n^+ source and drain wells have been confirmed by modeling of similar 6H-SiC MESFETs at high frequency. The RF performance potential of 6H-SiC MESFETs at 0.5, 3, and 10 GHz was investigated. Making conservative assumptions for mobility and contact resistance values, 240 cm^2/V-sec and 1 x 10^{-4} Ω-cm^2 respectively, and assuming n^+ source and drain wells, maximum power was calculated for each of these frequencies. The assumed dimensions of the device were a 1 μm gate length, a 1 μm source-gate distance, and a 2 μm gate-drain distance. The 6H-SiC devices produced about 630 W, 158 W and 45 W at those three frequencies, respectively. This corresponds to a normalized RF output power of about 2.5 W/mm of gate length. This value compares quite favorably with the 0.5-0.6 W/mm obtained with GaAs power FETs. Power-added efficiency and gain were also quite good and are shown, along with output power, as a function of frequency in Figure 13. All devices were biased for class A operation and CW

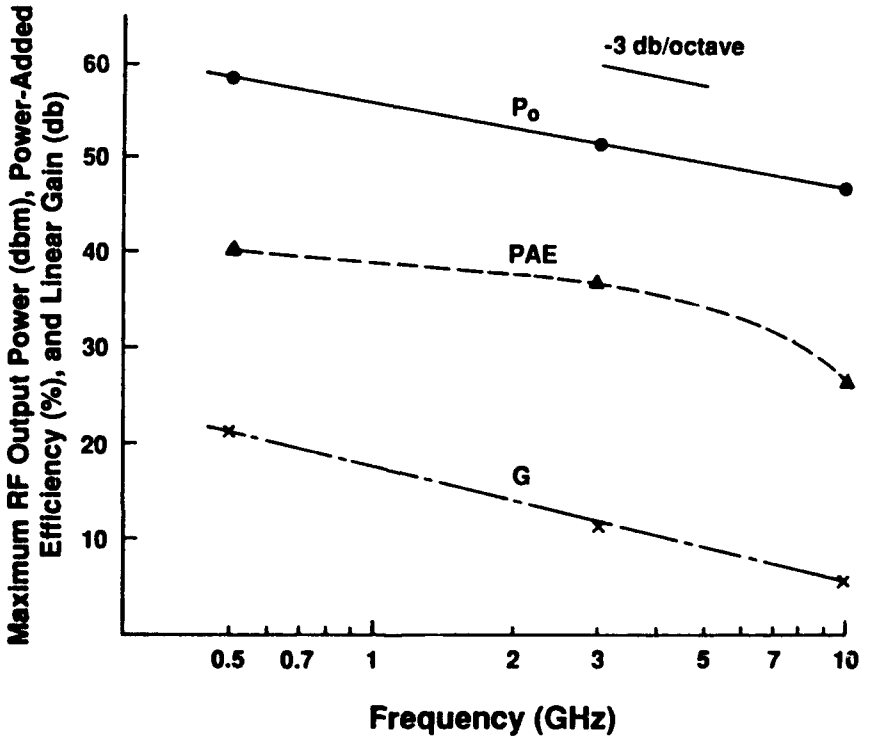

Figure 13. Modeled maximum RF performance as a function of frequency for 6HSiC MESFETs (V_{DS} = 40 V, I_{DS} = I_{DSS}/2, L_g = 1 μm). RF output powers of 630 W, 158 W, and 45 W were obtained at 0.5, 3, and 10 GHz, respectively.

conditions were assumed. Increased output power could be obtained from class B or C operation and/or pulse bias conditions; however, these modes of operation were beyond the scope of this investigation. Due to the excellent thermal conductivity of SiC, thermal modeling of the MESFETs showed that they are not thermally limited and should, in fact, be operable at elevated temperatures.

The DC transconductances observed for the devices discussed above were quite low when compared to other long gate length MESFET devices fabricated at Cree, considering the much smaller gate lengths and source-drain distances used in the high frequency design. This indicated that the limiting parasitic resistance is not related to mobility between the source and drain, but rather to contact resistance at the source and drain. It was apparent that the source and drain resistance are so dominant that the effect of reducing the gate length and source-drain spacing on the DC transconductance was negligible. The device modeling described above further proved this to be true. The modeled channel resistances were in the range of 35 Ω, while the measured resistances were more in the range of 110 - 130 Ω. Thus, as noted above the next iteration of 6H-SiC MESFETs was fabricated with n^+ source and drain wells, as was discussed in the previous section. This not only greatly reduced the resistivity of the SiC, but also greatly reduced the contact resistance of the ohmic contacts. The measured channel resistance of the devices with the n^+ source and drain wells were very close to the modeled resistances having values ranging from 30 - 37 Ω.

A typical DC current-voltage plot of one of these 6H-SiC MESFETs with an n^+ source and drain is shown in Figure 14. This device had a gate length and width of 1.8 μm and 1 mm, respectively. Drain voltages of 20 V were achieved with relatively good current saturation; higher drain voltages resulted in a detrimental increase in source/drain leakage current. These characteristics show a very good match with the modeling for a 1.8 μm device up to V_D = 10 V, where the effects of source/drain leakage current and gate leakage current begin to show. This match is very encouraging, indicating that the modeling for the optimal devices that was performed should be quite accurate. The DC power output of this device was about 5 W/mm of gate width. The maximum transconductance of this device was 17 mS/mm at V_D = 20 V and V_G = 0 V, and the measured channel resistance was 33.4 Ω. The gate leakage current at V_D = 20 V and V_G = -15 V was 1-2 mA, which is much larger than gate leakage currents observed in previous MESFET devices. This increased leakage current, as well as increased source-drain leakage current, is thought to be due to the sample having a higher defect density than wafers that were used previously.

The positive benefits of n^+ source and drain wells were also confirmed by measurement of the 6H-SiC MESFETs at high frequency. This device was measured at high frequency using an HP 8510 automatic network analyzer with a Cascade Microprober

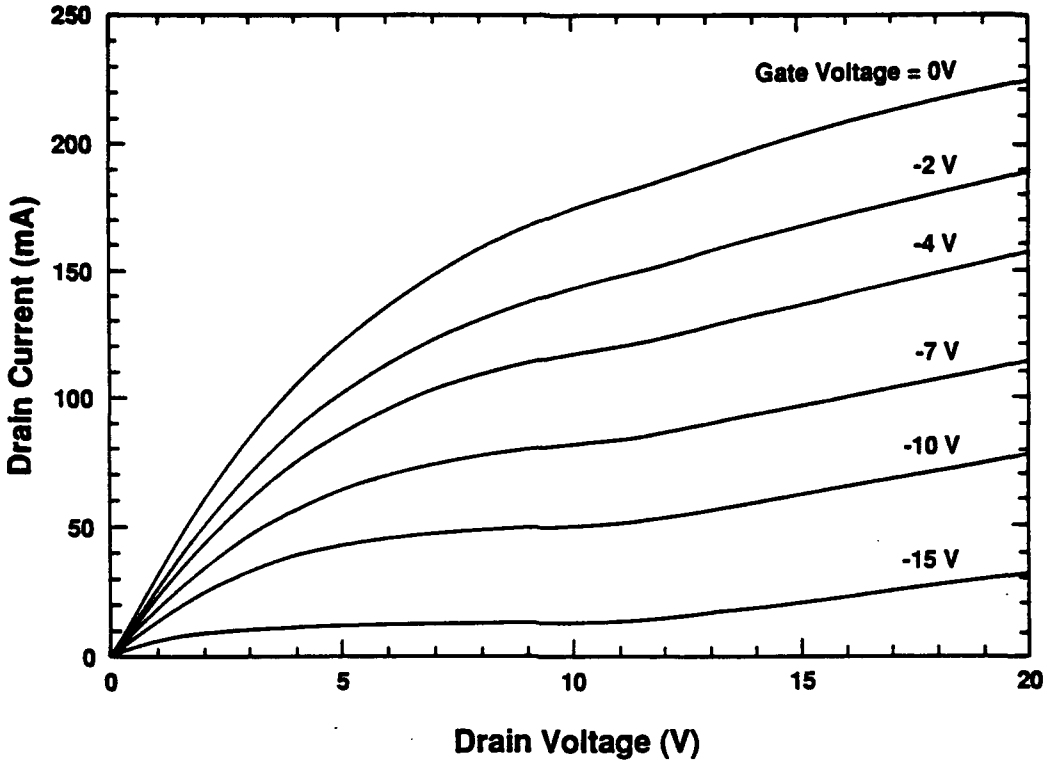

Figure 14. Drain current-voltage characteristics of a SiC MESFET using high power high frequency mask. Gate length and width are 1.8 μm and 1 mm, respectively. Source-drain distance is 4 μm. The maximum transconductance is 17 mS/mm.

for standard S-parameter measurements. The plot in Figure 15 shows that this device has a threshold frequency (F_t) of 1.35 GHz, designated where the H21 parameter crosses 0 dB gain. The device has an F_{max} of 500 MHz, where the power gain (G_{max}) crosses 0 dB gain. The previously observed average values for F_t and F_{max} were 600 MHz and 380 MHz, respectively.

While the DC characteristics of this device were very close to the modeled characteristics, the high frequency measurements were not. The modeling for the 1.8 μm gate length showed that the device should have had an 11 dB gain at 3 GHz (see section on MESFET modeling). Obviously, there was still a very large parasitic present in the device that greatly reduced the high frequency gain. Initially, it was thought that the "killer" parasitic was the gate capacitance due to the gate contact pad. The total gate capacitance measured was 5.75 pF. Of this capacitance, only about 1.7 pF was due to the area of the Schottky gate contact, with the other 4 pF arising from the 300 nm thick Si_3N_4 isolation pad. Thus the gate capacitance was 3.4 times higher than the modeling assumed. However, when the modeling calculations were performed with this higher gate capacitance, the high frequency performance was not degraded enough to account for the measured high frequency parameters.

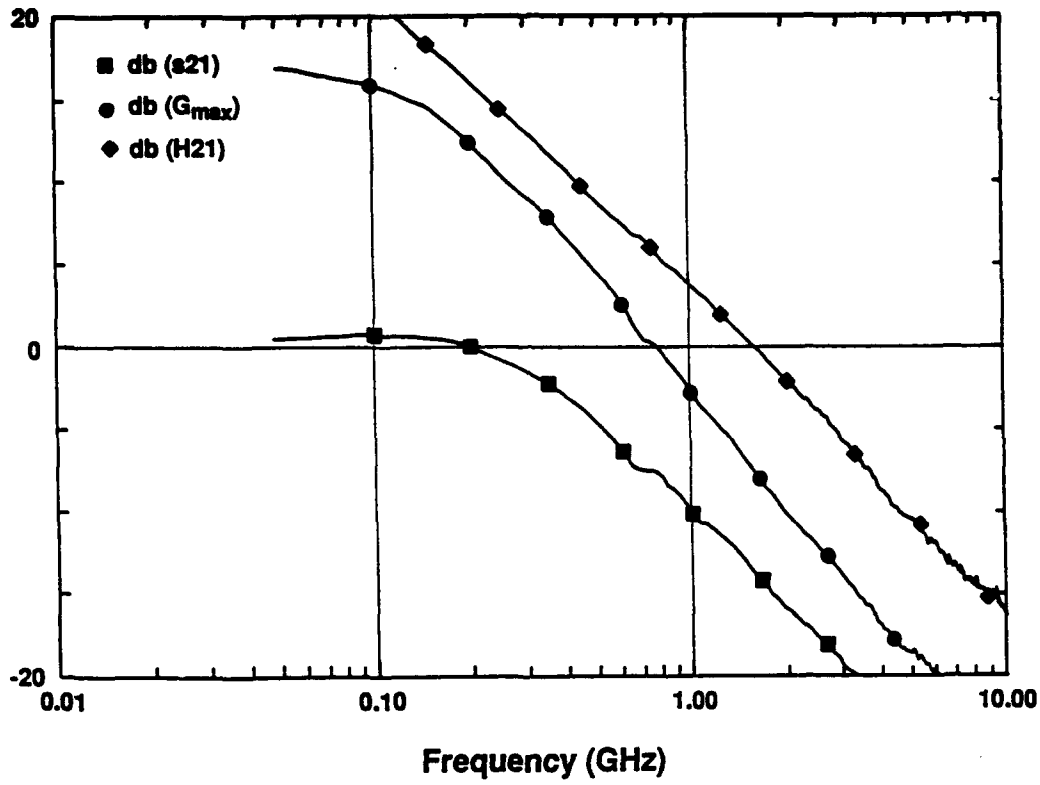

Figure 15. High frequency parameters, S21, G_{max}, and H21, as a function of frequency for the 1.8 μm gate length device shown in Figure 16. Measurement conditions were V_D = 20 V, I_D = 252 mA, V_G = 0 V, and I_G = 142 μA.

The next parasitic that was addressed was the gate resistance. The gates of these devices were very thin (100 nm). Given this very small cross-section and the long finger length (500 μm), the series resistance along the gate fingers was very high, with values in the range of 150 -300 Ω. When the modeling was performed using this high gate resistance, the high frequency gain was severely degraded to values that were very close to those that were measured. For GaAs MESFETs, it has been found that 10 Ω of gate resistance is a "critical" value to avoid serious parasitic effects, with a preferred value of 1.5 Ω. These low values of gate resistance are achieved by using thick overlayers of gold (which has a very low resistivity) on top of the gate contacts.

In order to confirm the effects of gate resistance on the high frequency parameters, an overlayer was deposited on top of the gate contact of the same device shown in Figures 14 and 15. Since gold was not available at the time, and it was not certain that a thick layer could be "lifted off," a 200 nm thick overlayer of Al was deposited instead. While far from optimal, a significant reduction in gate resistance did result from this overlayer. This overlayer actually caused an unexpected noticeable improvement in the DC characteristics of the device. The I-V characteristics shown in Figure 16 show that the current saturation was slightly improved and the maximum transconductance increased from 17 mS/mm to

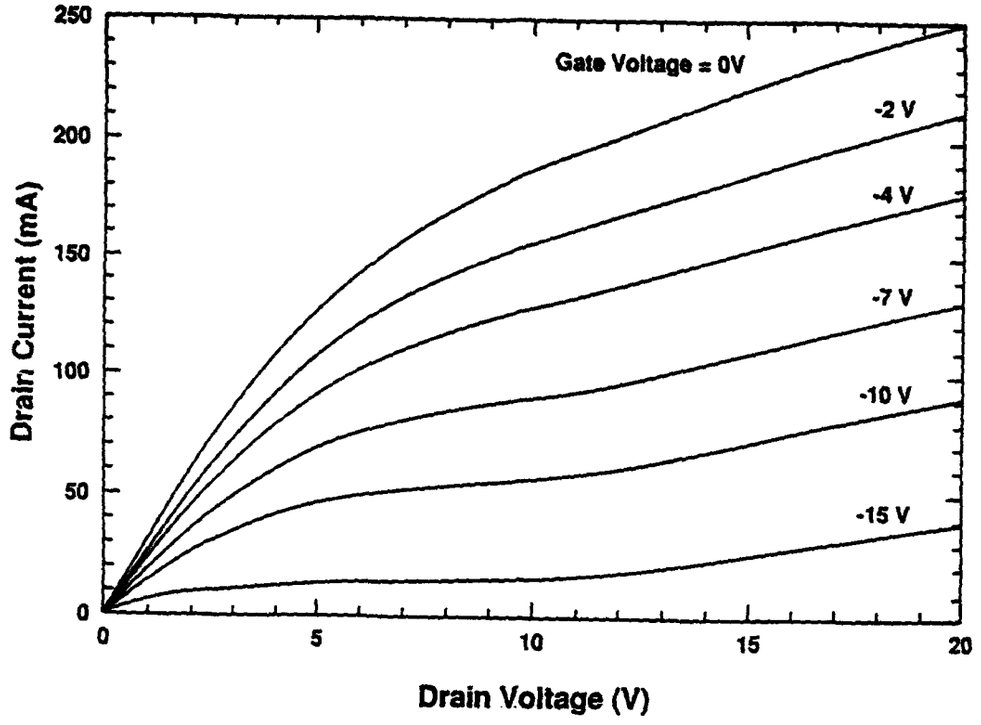

Figure 16. Drain current-voltage characteristics of the same SiC MESFET shown in Figures 14 and 15 after deposition of a 200 nm thick Al overlayer on the gate. The maximum transconductance is 18 mS/mm.

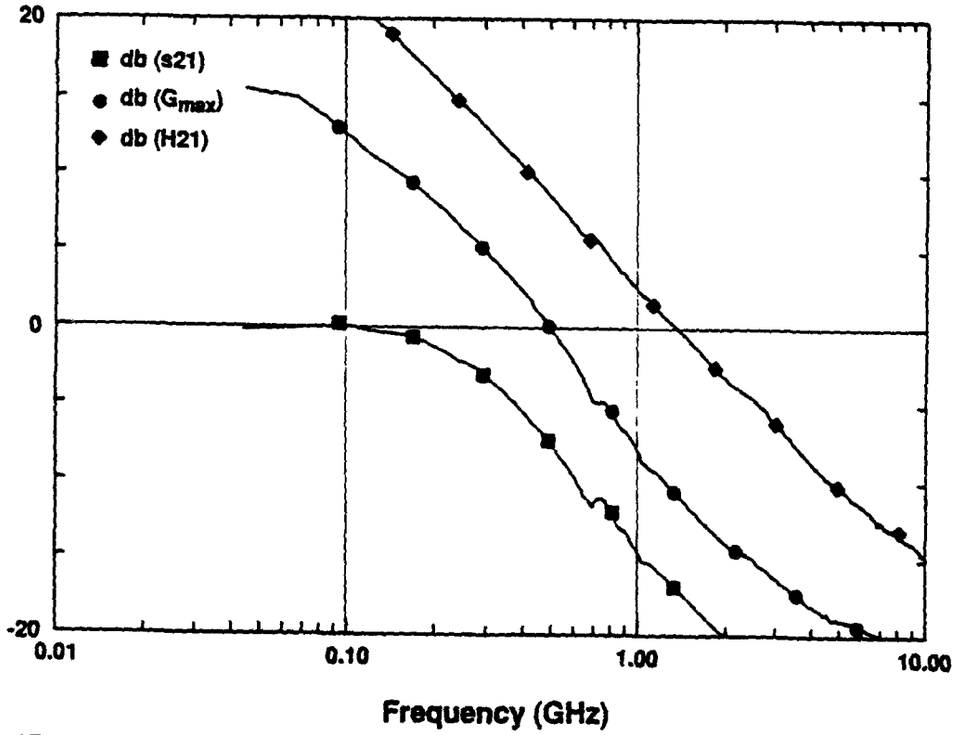

Figure 17. High frequency parameters, S21, G_{max}, and H21, as a function of frequency for the device in Fig. 3 with the Al gate overlayer. Measurement conditions were V_D = 20 V, I_D = 240 mA, V_G = 0 V, and I_G = 123 μA.

18 mS/mm. A gain vs. frequency plot for the same device with the Al overlayer is shown in Figure 17. The F_{max} of this device showed a marked increase from 500 MHz to 770 MHz, and the F_t increased from 1.35 GHz to 1.6 GHz. At 500 MHz, the device had a power gain of 4.6 dB and a current gain of 8.5 dB.

The major issues to be addressed were to minimize the same parasitics that have to be dealt with in any high frequency device in any material, primarily gate resistance and gate capacitance, and to further reduce the gate length for higher gain. The results of this effort are described in the following parahraphs.

The problems of gate resistance and gate capacitance were addressed in using the device structure shown in Figure 4. The research was very successful in both areas. In terms of parasitic gate capacitance, the value was reduced from 5.75 pF to 1.9 pF. This was due to the smaller area gate contact pad and the use of deposited SiO_2 as the pad isolation material. The SiO_2 was used because of its low dielectric constant of 3.9 as compared with that of Si_3N_4 (7.5), which was used in earlier devices.

Using the excimer laser stepper, sub-micron lines were achieved for the first time in SiC. The minimum gate length acheived was between 0.6 and 0.7 μm (the intended gate length was 0.6 μm). The smallest gate length that had been achieved previously was about 1.7 μm. Furthermore, overlayers of gold as thick as 750 nm were deposited on top of the gates. The laser stepper also allowed a much higher yield of devices per wafer.

A typical DC current-voltage plot of one of these 6H-SiC MESFETs fabricated with the new mask is shown in Figure 10. This device had a gate length and width of 0.7 μm and 1 mm, respectively. Although this device had a breakdown voltage at V_D = 14 V, other devices demonstrated drain voltages as high as 45 V. The maximum transconductance of this device was 25 mS/mm at V_D = 20 V and V_G = 0 V, and the measured channel resistance was 39 Ω. The pinch-off voltage was at V_G = -8.5 V. The gate leakage at V_G = -1.5 V and V_D = 14 V was 363 μA, but increased to 5 mA at V_G = -9 V and V_D = 14 V, which is quite high. This device had a 600 nm thick gold overlayer on the gate.

The positive benefits of the reduced gate length were made apparent by measurement of the 6H-SiC MESFETs at high frequency. This device was measured at high frequency using an HP 8510 automatic network analyzer with a Cascade Microprober for standard S-parameter measurements. The plot in Figure 19 shows that this device has a threshold frequency (F_t) of at least 2.9 GHz. Although the H_{21} parameter actually crosses 0 dB gain at 3.5 GHz, there is some curvature to the slope that makes this value unreliable. Therefore, the value of F_t =2.9 GHz was derived by extrapolation of the lower frequency data. The device has an F_{max} of 1.8 GHz, where the power gain (G_{max}) crosses 0 dB gain. The previously observed average values for F_t and F_{max} were 1.6 GHz and 770 MHz, respectively.

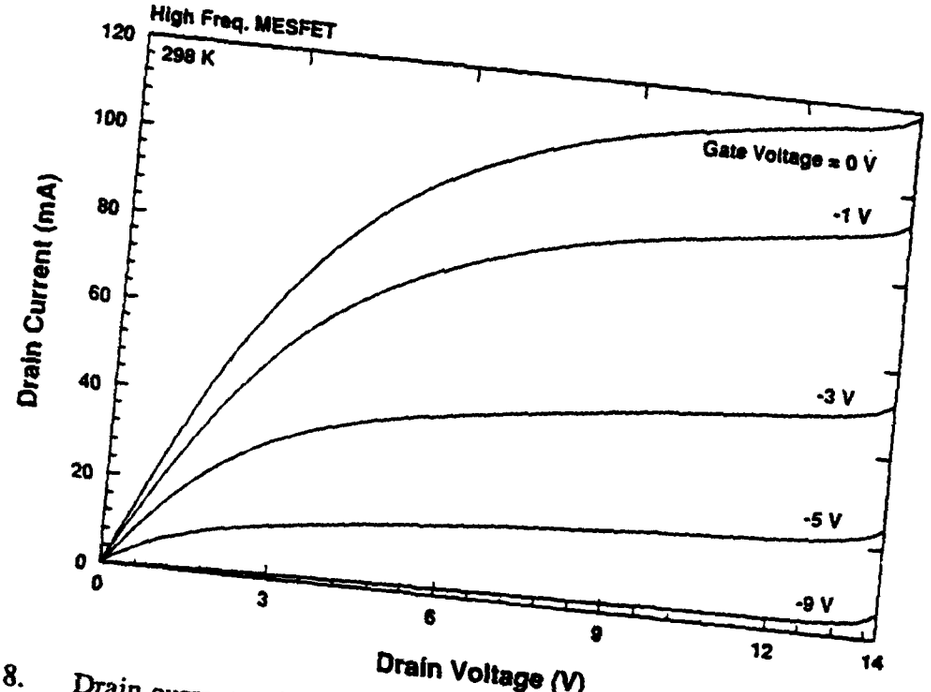

Figure 18. Drain current-voltage characteristics of a SiC MESFET. Gate length and width were 0.7 μm and 1 mm, respectively. Source-drain distance was 2.1 μm. The maximum transconductance was 25 mS/mm.

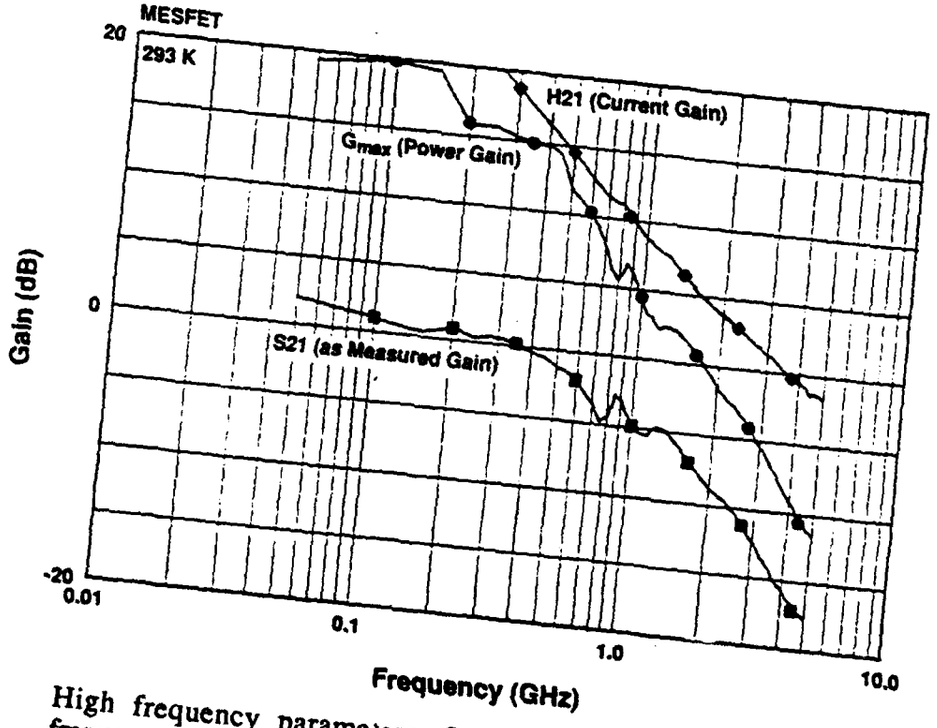

Figure 19. High frequency parameters, S_{21}, Gmax, and H_{21}, as a function of frequency for the 0.7 μm gate length device. Measurement conditions were V_D = 14 V, I_D = 81 mA, V_G = -1.5 V, and I_G = 363 μA.

The DC current-voltage plot in Figure 20 shows another 6H-SiC MESFET device that has higher drain voltage capability. This device also had a gate length and width of 0.7 μm and 1 mm, but it had a thicker gold overlayer of 750 nm. This device showed good current saturation out to 35 V and a non-destructive breakdown of the SiC at V_D = 37 V. The maximum current for this device was only 50 mA because the channel thickness was not as thick as it should have been, as evidenced by the pinch-off voltage of V_G = -4.5 V and the measured source-drain resistance of 67 Ω. The maximum transconductance of this device was 19 mS/mm at V_G = 0 V. The gate leakage current at V_G = 0 V and V_D = 33 V was 385 μA, and increased to 800 μA at V_G = -4.5 V.

A gain vs. frequency plot for the same device with the 750 nm overlayer shown in Figure 20 is shown in Figure 21. As was expected, the F_t of 2.4 GHz was lower than the previously discussed device because of the much higher source-drain resistance. However, despite the higher resistance, the F_{max} of 1.9 GHz was even higher than the previous device. It is proposed that the thicker gate overlayer (25% thicker) caused sufficient drop in the parasitic gate resistance to overcome the effects of the higher source-drain resistance. At 1.0 GHz, the device in Figure 19 had a power gain of about 4.5 dB and a current gain of 8.5 dB. The device in Figure 21 with reduced gate resistance had a power gain and a current gain of 7.0 dB each at 1.0 GHz. Based on these results, it was apparent that the gate resistance is by far the most important parasitic to be addressed.

While these were marked improvements in high frequency operation, they were somewhat lower than first expected, since the gate lengths were reduced by almost 60% over devices that were fabricated in previous batches. However, for every reduction in gate length, there must be an equivalent increase in gate overlayer thickness to maintain the same cross-sectional area and same gate resistance. The gates of these devices were still not thick enough at 750 nm. Given the very small cross-section and the long finger length (500 μm), the series resistance along the gate fingers still have values in the range of 35-40 Ω. For GaAs MESFETs, it has been found that 10 Ω of gate resistance is a "critical" value to avoid serious parasitic effects, with a preferred value of 1.5 Ω. These low values of gate resistance are achieved by using thick overlayers of gold on top of the gate contacts, quite often employing techniques that enlarge the cross-sectional area (mushroom gates).

In order to reduce the source resistance, the channel thickness of subsequent devices was increased, allowing pinch-off voltages of -10 V or more. Also, the best of the new wafers utilized ion implanted source and drain wells instead of the "mesa-style" MESFETs. It is assumed that the ion implanted wells result in a lower source and drain resistance because of the ability to dope to very high levels with implantation. Also, as noted above, a thicker gold overlayer (1 μm) was used to reduce gate resistance, and a thicker isolating SiO_2 layer (1 μm) was employed to reduce gate capacitance.

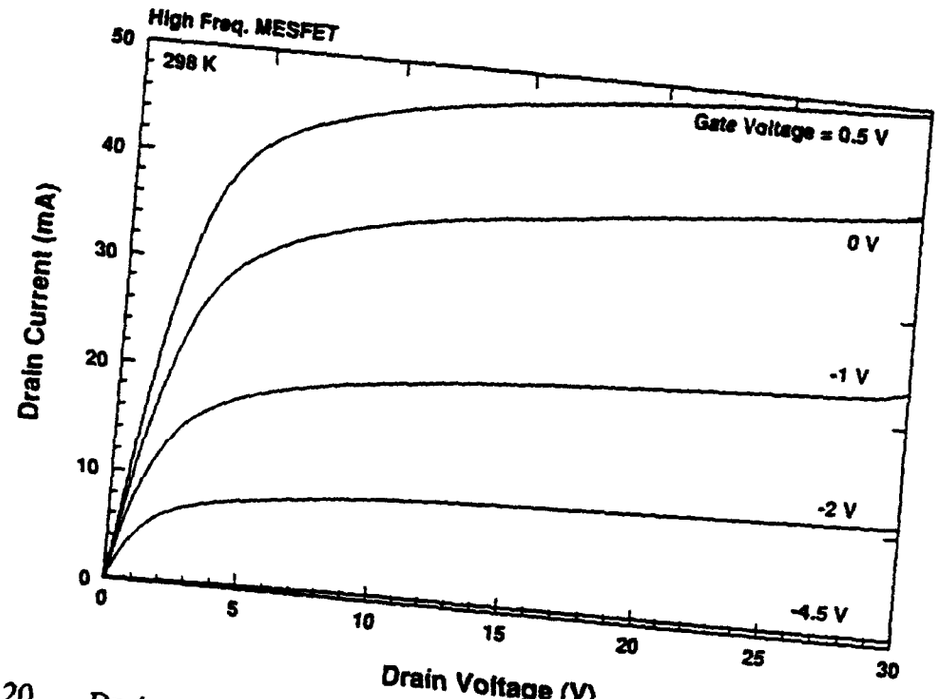

Figure 20. Drain current-voltage characteristics of a 6H-SiC MESFET with a thicker gold gate overlayer (750 nm). Gate length and width were 0.7 μm and 1 mm, respectively. Source-drain distance was 2.1 μm. The maximum transconductance was 19 mS/mm.

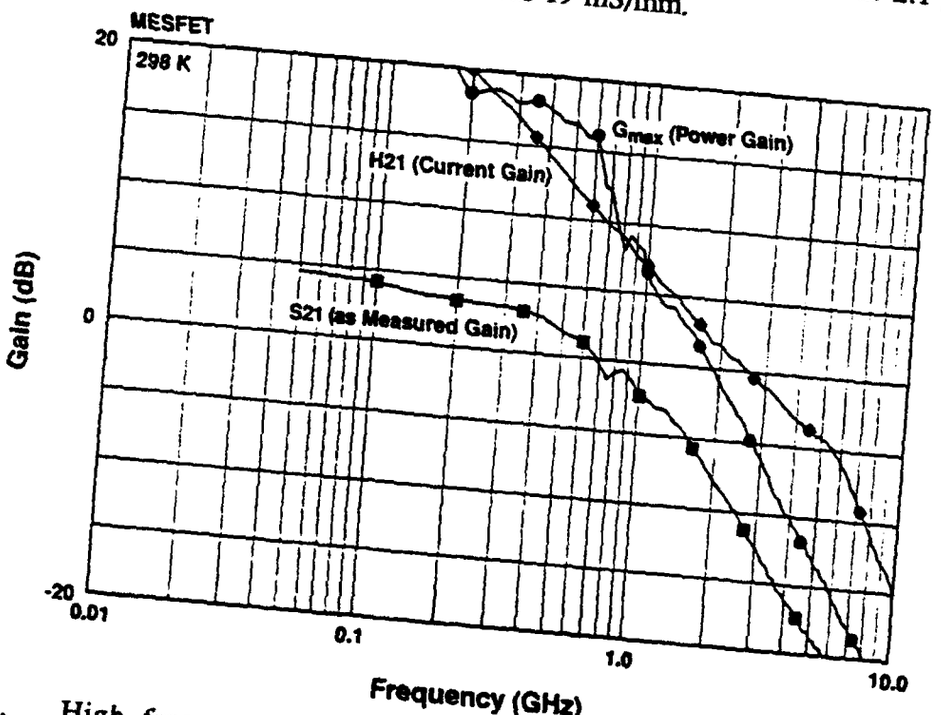

Figure 21. High frequency parameters, S_{21}, G_{max}, and H_{21}, as a function of frequency for the device shown in Figure 20. Measurement conditions were $V_D = 33$ V, $I_D = 50$ mA, $V_G = 0$ V, and $I_G = 385$ μA.

A typical current-voltage plot, obtained from a 60 Hz curve tracer, of one of these 6H-SiC MESFETs is shown in Figure 22. This device had a gate length and width of 0.6 μm and 1 mm, respectively, and had a breakdown voltage at V_D = 50 V. The maximum transconductance of this device was about 25 mS/mm at V_D = 40 V and V_G = 0 V, and the measured channel resistance was 43 Ω. The gate leakage at V_G = 0 V and V_D = 40 V was about 350 μA. The drain on-current at V_G = 0 V (I_{DSS}) was 310 mA/mm with a pinch-off voltage (V_{po}) of V_G = -17 V. By achieving this I_{DSS} at V_D = 40 V, the corresponding DC power density of this device was 12.4 W/mm. This power level is two to three times higher than can be achieved with equivalent GaAs or Si devices.

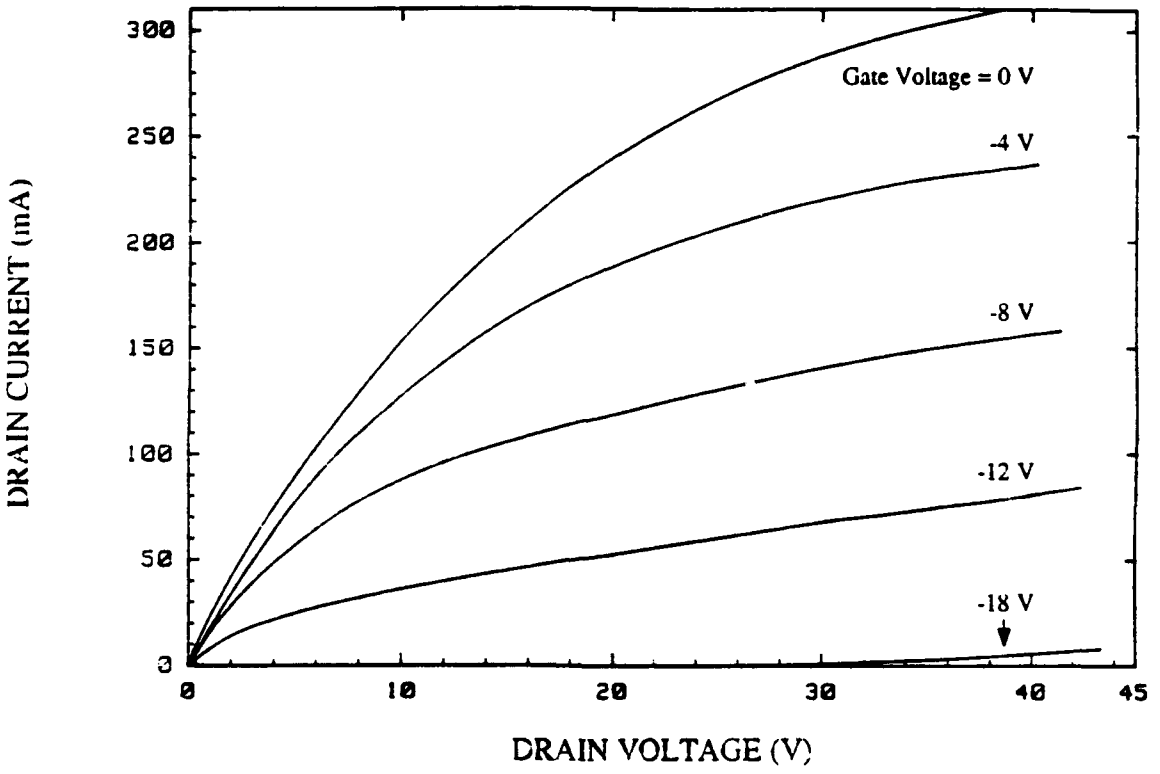

Figure 22. Drain current-voltage characteristics (at 60 Hz) of a high frequency 6H-SiC MESFET. Gate length and width are 0.6 μm and 1 mm, respectively. Source-to-drain length is 2.9 μm.

This device was measured at high frequency using an HP 8510 automatic network analyzer with a Cascade Microprober for standard S-parameter measurements. The plot in Figure 23 shows that this device had a threshold frequency (f_t) of about 4.5 GHz, where the H_{21} parameter crosses 0 dB gain. The device had a maximum frequency (f_{max}) of about 3.0 GHz, where the power gain (G_{max}) crosses 0 dB gain. At 1.0 GHz, this device had a power gain and a current gain of 13.5 dB and 12.5 dB, respectively. While RF power measurements were not performed on these devices, it is anticipated that significant RF power output will be achieved at 1 GHz.

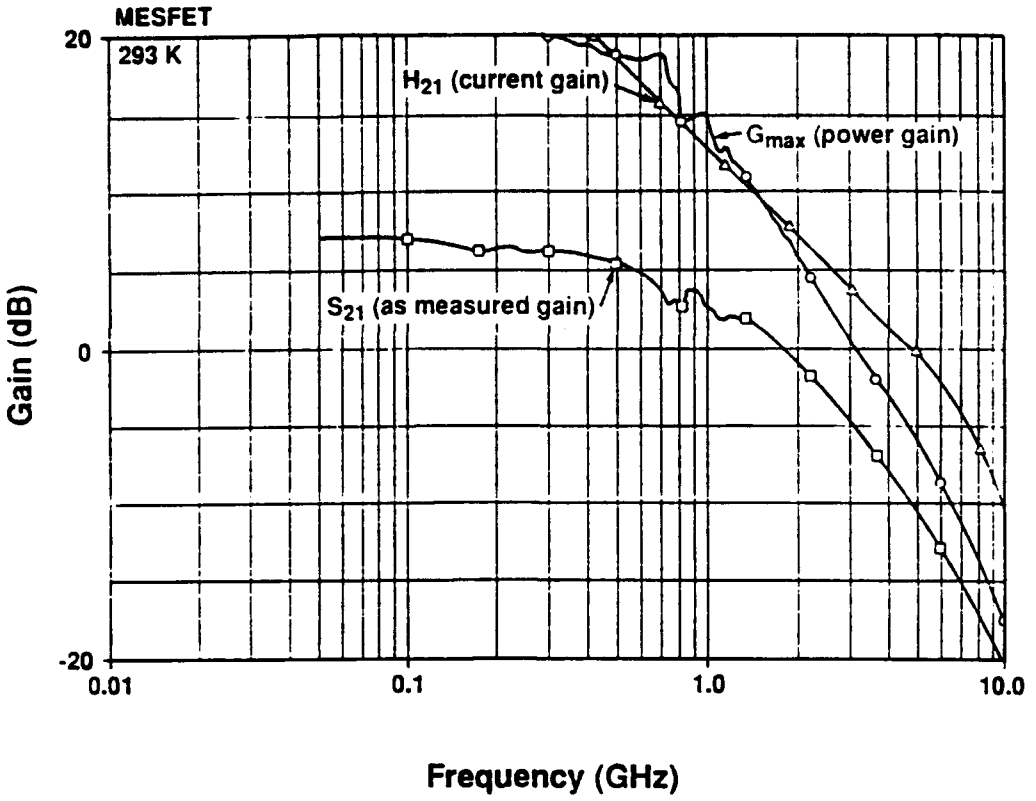

Figure 23. High frequency parameters, S_{21}, G_{max}, and H_{21}, as a function of frequency for the 0.6 μm gate length device shown in Figure 4. Measurement conditions were V_D = 35 V, I_D = 260 mA, V_G = -3.0 V, and I_G = 258 μA.

It is obvious from the I-V curves that these SiC devices can operate at extremely high drain and gate biases (40 V) for submicron devices as compared with the 5-10 V typically achievable with submicron GaAs devices. Therefore, it is easy to see that SiC MESFETs should be able to operate at much higher power levels than GaAs. While there are also marked improvements in high frequency operation, they are still somewhat lower than desired. However, there is still much room for improvement of the high frequency parasitics in these devices. The gate overlayers of these devices are still not sufficiently thick at 1.0 μm. Given the very small cross-section and the long finger length (500 μm), the series resistance along the gate fingers still had values in the range of 10-20 Ω. For GaAs MESFETs, it has been found that 10 Ω of gate resistance is a "critical" value to avoid serious parasitic effects, with a preferred value of 1.5 Ω. These low values of gate resistance are achieved by using thick overlayers of gold on top of the gate contacts, quite often employing techniques that enlarge the cross-sectional area (eg., mushroom gates).

IMPATT Diode Characterization. The initial modeling for IMPATT diodes was for operation at 60 GHz using a flat profile for the drift layer, and showed that this epilayer must have $n = 4 \times 10^{16}$ cm^{-3} and a thickness of 2 μm. This thickness and carrier concentration are dictated by that desired frequency. However, none of the structures

showed promising avalanche characteristics, because of the amount of sub-avalanche reverse bias leakage current due to passivation problems. Most of the devices had a leakage current of about 1 mA at a reverse bias of 30 V, which was well below the avalanche voltage. Therefore, further efforts focused on using a "high-low" structure (see Figure 5), which would keep the avalanche voltage low and decrease the sidewall passivation requirements. These "high-low" structures were made using both a pn junction diode and a Schottky diode.

The p-n junction high-low IMPATT structures showed very low reverse bias leakage currents. The I-V characteristics of a p-n junction high-low IMPATT diode ($A = 8.11\times10^{-5}$ cm^{-2}) shown in Figure 24 showed a very low reverse bias leakage current out to about -90 V followed by a sharp avalanche breakdown with a negative resistance slope. The average leakage current at V = -80 V was 80 nA; at V = -50 V, the leakage current was about 2 nA ($J = 2.5\times10^{-5}$ A/cm^2). The avalanche current of this device exceeded 105 mA, corresponding to an avalanche power density of about 120 kW/cm^2. This is a very high power density and it is expected that the junction temperature at this power level is quite high. Indeed, further increases in avalanche current began to degrade the performance of the device.

The reverse bias avalanche characteristics of a different, smaller IMPATT device are shown on an expanded scale in Figure 25. This device, which had an area of 4.56×10^{-5} cm^2, again showed very low leakage current below avalanche at about 97 V. More importantly, the negative resistance of this device was observed as the avalanche current was increased. The maximum negative resistance of this device was about -63 Ω. This corresponds to a negative conductance of -348 $mhos/cm^2$. This value of conductance was similar to that normally observed for Si and GaAs IMPATT diodes, which operate within the range of 200-700 $mhos/cm^2$. It is important to note that this value is for a SiC diode that is not thinned (substrate is ≈200 μm thick), therefore there is a large passive resistance associated with the substrate. In addition, the contact resistance also contributes a large passive resitance component. Thus, the intrinsic negative resistance of the devices is likely to be twice as high as the measured value.

The avalanche current of 59 mA at 96 V for the device shown in Figure 25 again corresponds to a very high avalanche power density of 124 kW/cm^2. Good avalanche characteristics were observed for other devices with higher breakdown voltages, showing avalanche currents as high as 5 mA at 295 V. However, this corresponds to only 15% of the avalanche power density observed for the lower voltage devices and the yield for the high voltage devices was lower also.

The forward bias I-V characteristics of the IMPATT diode shown in Figure 25 are shown in Figure 26. The diode has a turn-on voltage of about 2.6 V and has a forward

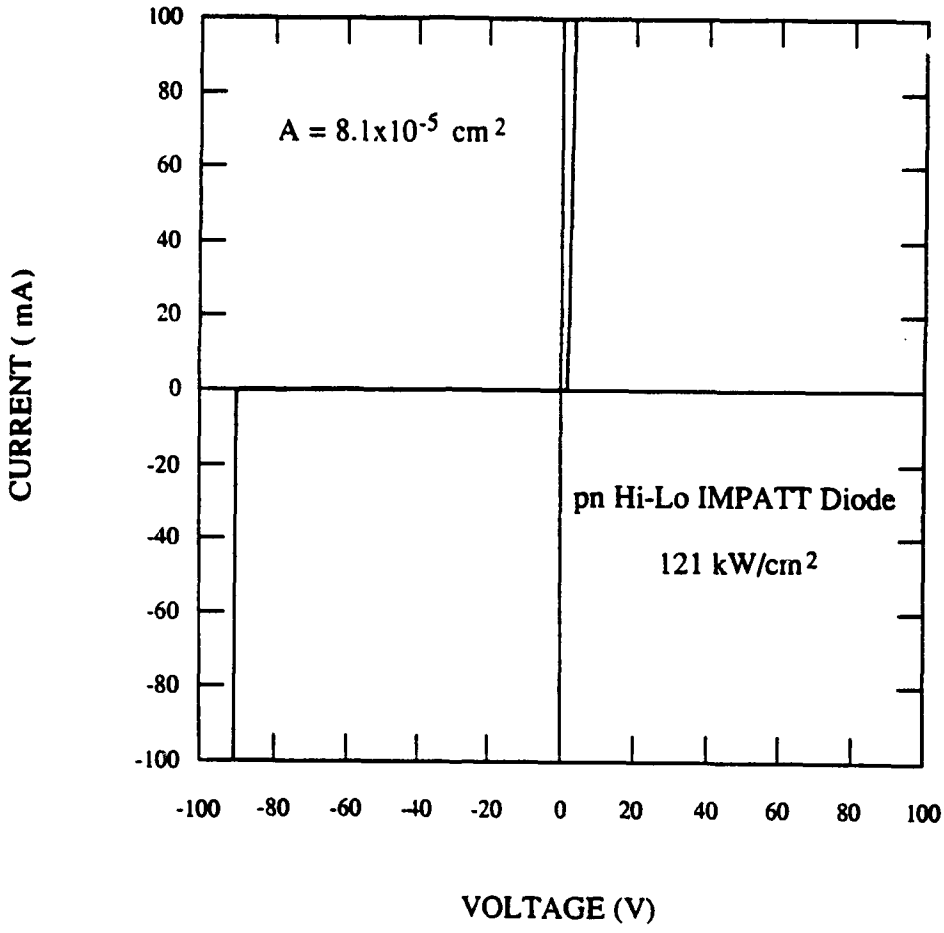

Figure 24. Current-voltage characteristics of a 6H-SiC p-n junction "high-low" IMPATT diode structure. The junction area was 8.1×10^{-5} cm^2.

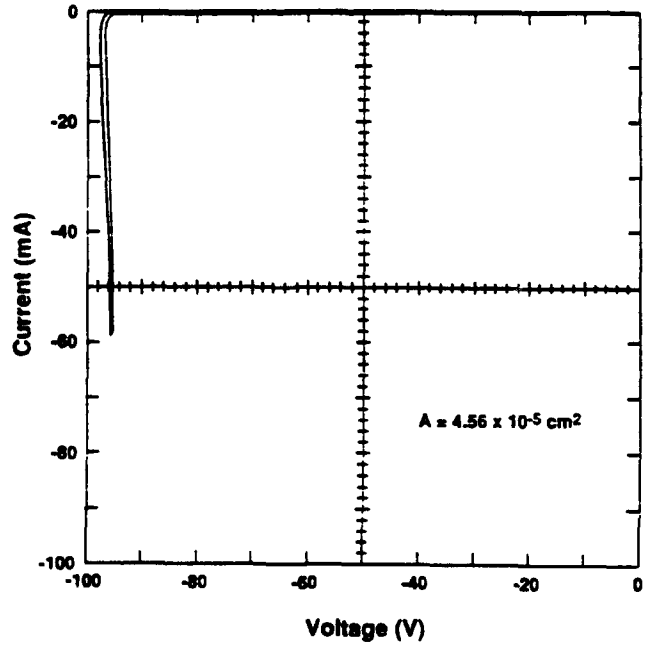

Figure 25. Reverse bias I-V characteristics of a different 6H-SiC p-n junction "high-low" IMPATT diode structure. The junction area was 4.56×10^{-5} cm^2. Note the -63 Ω negative resistance in avalanche and the 124 kW/cm^2 DC avalanche power density.

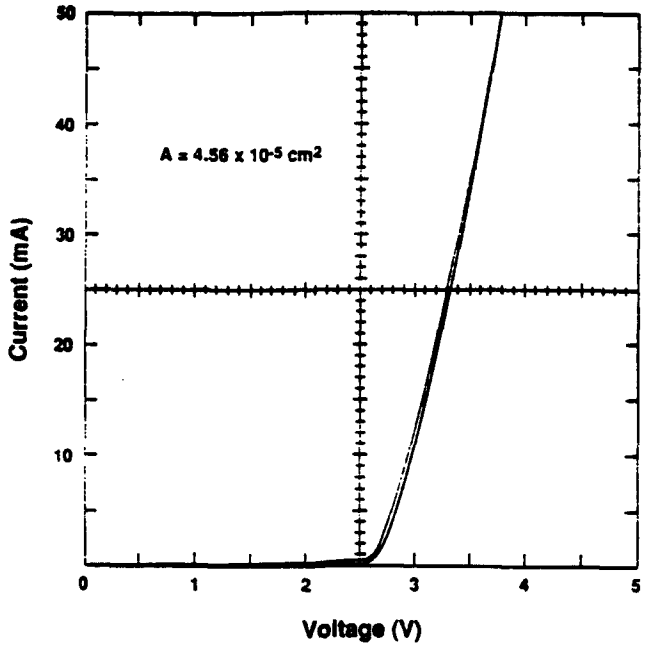

Figure 26. Forward bias I-V characteristics of the same p-n junction "high-low" IMPATT diode shown in Fig. 25. Note the 18 Ω forward bias resistance.

current of 50 mA at about 3.5 V. Thus, the diode had a forward resistance of about 18 Ω, or 8.2×10^{-4} Ω-cm^2. Using known bulk resistivities and ohmic contact resistivities for 6H-SiC, the component of the resistance due to the substrate was calculated to be about 5.4 Ω. The p-type ohmic contact resistance was calculated to be about 9.0 Ω (2.2×10^{-4} Ω-cm^2) and the resistance due to the low doped drift region was about 3.0 Ω. Finally, the n-type ohmic contact was calculated to be about 0.6 Ω, resulting in a total resistance of 18 Ω. If a 6H-SiC IMPATT diode was fabricated with a thinned substrate and backside contact vias, then the substrate resistance could be ignored. However, the p-type ohmic contact resistance would contribute about 72% of the resistance.

Therefore the purpose of the next batch of IMPATT diode wafers was to greatly reduce the p-type ohmic contact resistance. The most obvious method of achieving lower contact resistance was to increase the p-type doping level. If the carrier concentration of the p$^+$ layer could be increased from the 5×10^{18} cm^{-3}, obtained with the previous diodes, a concentration to $>2\times10^{19}$ cm^{-3}, the p-type ohmic contact resistance would be reduced by a factor of about three.

The wafers that were grown for this batch did have very heavy Al doping such that the carrier concentration was in the range of $1.5\text{-}2.5\times10^{19}$ cm^{-3}. While the resulting devices were quite conductive, they unfortunately showed much poorer I-V characteristics than the previous batch. The leakage currents began to increase dramatically above 30 V reverse bias. No desirable avalanche characteristics were observed for any of the wafers that were fabricated.

It is assumed that the difference between this batch and the last one lies in the very high Al doping level. By going to very high Al levels, there is a correspondingly high concentration of Al in the thermally grown SiO_2. It is proposed that the Al concentration in this present batch was so high that it degraded the insulating and passivating properties of the SiO_2 grown on the mesa exposed junction. Thus, a large amount of interfacial leakage current was generated at the junction around the periphery of the device when the reverse bias exceeded about 30 V.

The Schottky high-low IMPATT diodes that were fabricated in this study showed the first avalanche characteristics ever observed for a SiC Schottky device. The I-V characteristics shown in Figure 27 show that avalanche was achieved at a voltage of 43 V. Furthermore, the reverse bias leakage current was quite low, with a value of 2 μA at V = -20 V. This device had a diameter of 203 μm, therefore the leakage current translates to 6 mA/cm^2. The device had a sharp turn-on voltage in forward bias of 0.85 V, and forward current reached 200 mA at 1.9 V, which corresponds to a resistance of 5.25 Ω.

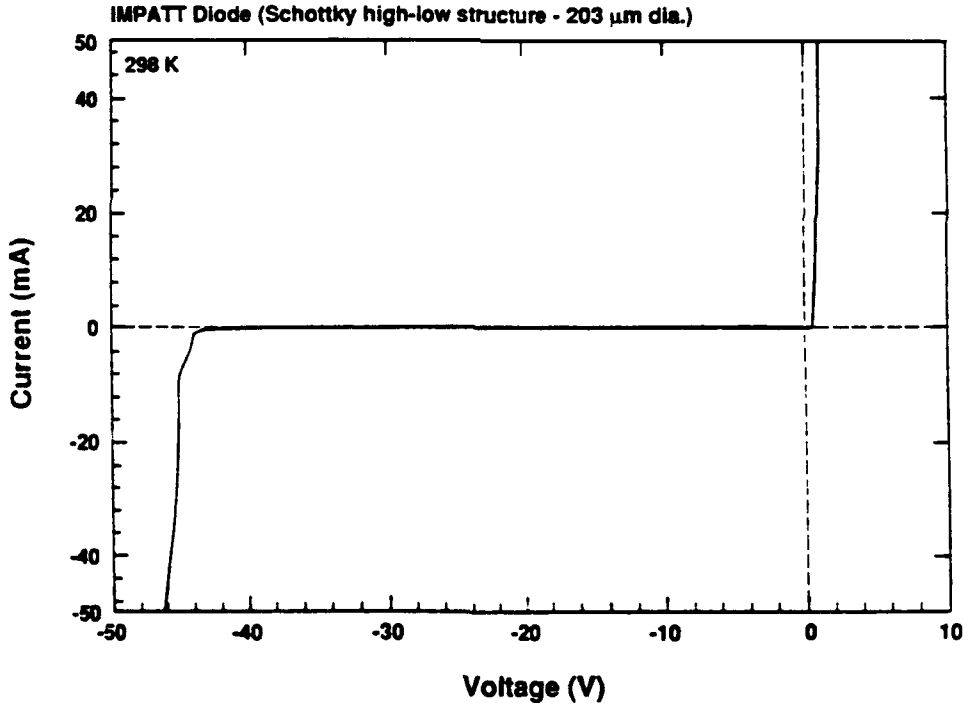

Figure 27. Current-voltage characteristics of a 6H-SiC Schottky barrier "high-low" IMPATT diode structure. Note avalanche current at reverse bias of -44 V.

The avalanche was also relatively sharp and had roughly the same slope as the forward bias current. This device withstood as much as 50 mA in avalanche current at 46 V, corresponding to an avalanche power density of 7.1 kW/cm^2. Another Schottky high-low device with a smaller diameter is shown in Figure 28. This device had a diameter of 102 μm. Although higher leakage current prevented the avalanche and forward turn-on from

being as sharp as the previous device, this device did show that a very high avalanche current density can be achieved with 6H-SiC. This device withstood more than 40 mA at 59 V, which corresponds to a very high avalanche power density of 29 kW/cm^2.

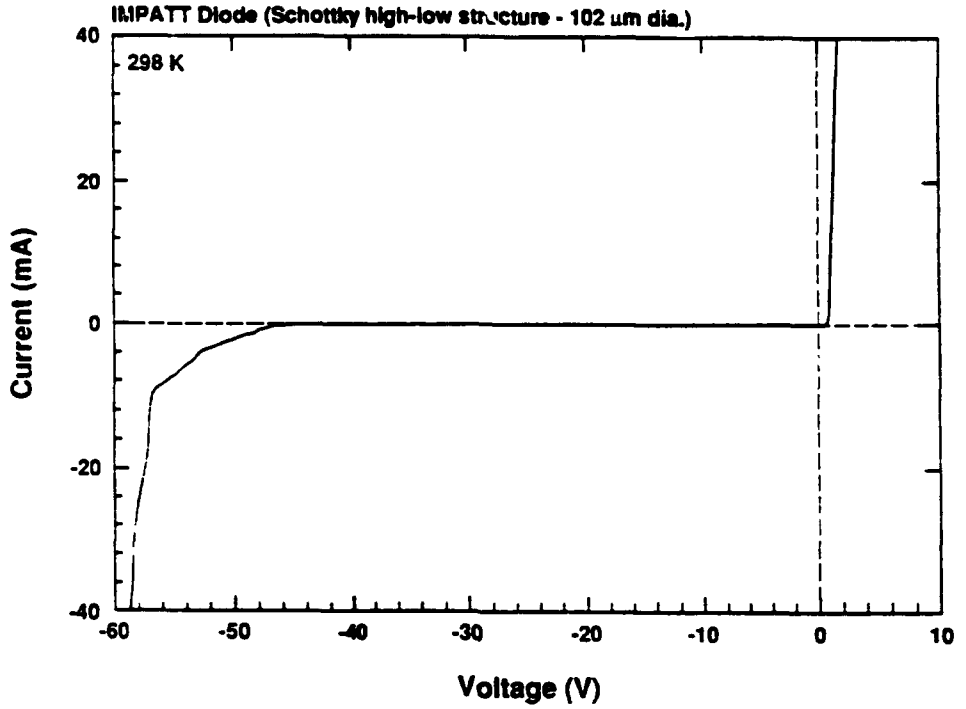

Figure 28. Current-voltage characteristics of 6H-SiC Schottky barrier "high-low" IMPATT diode structure. The avalanche current shown corresponds to a power density of 29 kW/cm^2.

While these Schottky-based IMPATTs seem to be the best structure to date, there is a very fundamental problem observed with these devices that will probably prevent them from being used for 60 GHz operation. The resistances of these diodes ranged from 4-20 Ω depending on the diameter of the device. Using known bulk resistivities and ohmic contact resistivities for 6H-SiC, the contact resistivity of the Schottky contact, an unknown until now, was calculated from the I-V characteristics. In forward bias, it appears that the Schottky contact contributes a contact resitivity of about 8×10^{-4} Ω-cm^2. Although the calculated value is not exact, it is a good estimation of the range of the contact resitivity. This level of resistance is about ten times higher than the ohmic contact to p-type material. Therefore, a pn junction-based IMPATT appears to be the most promising structure due to its lower overall resistivity.

D. Conclusions

High power / high frequency 6H-SiC MESFETs have been fabricated that show high gain at microwave frequencies, with the highest values for f_t and f_{max} being 4.5 GHz and

3.0 GHz, respectively. The measured DC power density was extraordinarily high, with a value of 12.4 W/mm. The main two parasitics that are currently limiting the high frequency behavior of these devices are source resistance and gate resistance.

Two different methods are being pursued to reduce the source resistance. These methods are 1) increasing the channel doping, and 2) use of recessed gate structures. Two different methods are being pursued to reduce the gate resistance. The first is to simply decrease the finger length by more than half. The second is to try to fabricate a "mushroom" style gate.

Avalanche characteristics for 6H-SiC p-n junction IMPATT diodes have been observed for the first time using a "high-low" doping structure. These devices showed avalanche power densities as high as 124 kW/cm^2. Additionally, they showed negative conductance in avalanche in the range of 348 mhos/cm^2. The forward bias resistances observed were in the range of 4.6-8.2$\times$10^{-4} Ω-cm^2, without substrate thinning. This value is approaching an acceptable range for high power operation at 60 GHz, the intended frequency for these IMPATT diodes. Based on the observed characteristics and the opportunity for improvement, the p-n junction based IMPATT appears to be a promising structure for high power microwave operation.

INDEX OF TECHNICAL REPORTS

Type of Report	Period Covered	Date of Report
Annual Letter Report	4/1/88–9/30/88	October 31, 1988
Semi-Annual Progress Report	10/1/88–6/30/89	July 31, 1989
Annual Letter Report	1/1/89–12/31/89	February 28, 1990
Semi-Annual Letter Report	1/1/90–6/30/90	July 1, 1990
Annual Letter Report	1/1/90–12/31/90	December 31, 1990
Semi-Annual Letter Report	1/1/91–6/30/91	June 30, 1991
Annual Letter Report	1/1/91–12/31/91	December 31, 1991
Semi-Annual Letter Report	1/1/92–6/30/92	June 30, 1992
Annual Letter Report	1/1/92–12/31/92	December 31, 1992
Final Technical Report	4/1/88–12/31/92	December 31, 1992

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